# STIC Search Report
## EIC 2100

STIC Database Tracking Number

| TO: | From: |
|---|---|
| Cynthia Britt<br>Location: RND 2D29<br>Art Unit : 2133<br>Tuesday, May 10, 2005<br><br>Case Serial Number: 10/068307 | Geoffrey St. Leger<br>Location: EIC 2100<br>Randolph-4B31<br>Phone: 23450<br><br>geoffrey.stleger@uspto.gov |

## Search Notes

Dear Examiner Britt,

Attached please find the results of your search request for application 10/068307. I searched Dialog's patent files and technical databases, along with the Internet and West.

Please let me know if you have any questions.

Regards,

Geoffrey St. Leger
4B31/x23540

# STIC Search Results Feedback Form

## EIC 2100

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact*:**

**Anne Hendrickson, EIC 2100 Team Leader**
**272-3490, RND 4B28**

## Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2133*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

*Types of relevant prior art found:*

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art **not found:***
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

**Comments:**

**Drop off or send completed forms to STIC/EIC2100 RND, 4B28**

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File 347:JAPIO Nov 1976-2005/Jan(Updated 050506)
         (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200529
         (c) 2005  Thomson Derwent

Set     Items   Description
S1       4426   "TEST"()DATA()IN OR TDI OR SCAN()IN
S2        616   "TEST"()DATA()OUT OR TDO OR SCAN()OUT
S3     198375   (INPUT OR NORMAL)()DATA OR DATA()IN
S4     119318   MULTIPLEX??? OR MULTIPLEX??? OR MUX???
S5      14271   DEMULTIPLEX??? OR DEMULTIPLEX??? OR DMUX??? OR DEMUX???
S6    1284938   SWITCH???
S7     142293   SCAN
S8      57221   CAPTUR???
S9     449967   RESPONSE
S10     31211   "TEST"()(VECTOR? ? OR PATTERN? ? OR BIT? ? OR BYTE? ? OR S-
              EQUENCE? ? OR SERIES OR STRING? ? OR DATA OR INFORMATION OR S-
              IGNAL? ? OR CHARACTER? ? OR INPUT? ?)
S11       320   S1 AND S2
S12         1   S11 AND S4 AND S5
S13      4606   "TEST"()DATA()(IN OR INPUT) OR TDI OR SCAN()IN
S14       739   "TEST"()DATA()(OUT OR OUTPUT) OR TDO OR SCAN()OUT
S15       370   S13 AND S14
S16         1   S15 AND S4 AND S5
S17        33   S15 AND S4
S18         1   S15 AND S5
S19        38   S15 AND S6
S20        56   (S17 OR S19) AND S7
S21         6   S20 AND S8:S9
S22     96730   (SECOND? OR 2ND)(3W)(S4 OR S6) OR (S4 OR S6)(3W)(2 OR TWO)
S23         8   S20 AND S22
S24     15111   PA=TEXI
S25         7   S15 AND S24
S26        10   S24 AND S13:S14 AND S7
S27        35   S24 AND S10 AND (S4:S6)
S28        11   S27 AND S8:S9
S29        20   S26 OR S28
S30         4   S10 AND S4 AND S5 AND S7
S31        52   S20 NOT S29:S30
S32        15   S31 AND BOUNDARY
```

29/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

016753620 **Image available**
WPI Acc No: 2005-077898/200509
XRPX Acc No: N05-068306
**Digital processors e.g. microprocessor, communication emulating method, involves supplying single start bit having digital state followed by preset data bits to test data input port for communication to boundary- scan architecture**
Patent Assignee: TEXAS INSTR INC ( **TEXI** )
Inventor: SWOBODA G L
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6836757 | B1 | 20041228 | US 99120667 | P | 19990219 | 200509 | B |
| | | | US 2000483321 | A | 20000114 | | |

Priority Applications (No Type Date): US 99120667 P 19990219; US 2000483321 A 20000114
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6836757 | B1 | | 10 | G06F-009/455 | Provisional application US 99120667 |

Abstract (Basic): US 6836757 B1

NOVELTY - The method involves supplying a serial signal having bits, to a **test data input** port for communication to boundary-**scan** architecture. Each bit of the signal has a digital state. A single start bit having another digital state followed by preset data bits is supplied to the port for communication to the architecture. The start bit is sensed within the architecture and the preset bits are stored.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a digital electronic module.

USE - Used for emulating communication between digital processors e.g. microprocessor, microcontroller and digital signal processor.

ADVANTAGE - The method easily emulates communication between the processors in real time. The method allows a user to control program execution, examine or change system memory and core CPU resources.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram form protocol multiplexing hardware.

Input and output switches (201, 202)
Serial **scan** path (204)
Start bit detector (210)
Processing core (220)
pp; 10 DwgNo 8/8

Title Terms: DIGITAL; PROCESSOR; MICROPROCESSOR; COMMUNICATE; EMULATION; METHOD; SUPPLY; SINGLE; START; BIT; DIGITAL; STATE; FOLLOW; PRESET; DATA; BIT; TEST; DATA; INPUT; PORT; COMMUNICATE; BOUNDARY; **SCAN** ; ARCHITECTURE
Derwent Class: S01; T01
International Patent Class (Main): G06F-009/455
File Segment: EPI

29/5/2 (Item 2 from file: 350)0
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

015738804 **Image available**
WPI Acc No: 2003-801005/200375
Related WPI Acc No: 2001-637686; 2002-391761; 2002-478804; 2004-429940
XRPX Acc No: N03-641899
**Integrated circuit has scan distributor circuit connected between one bond pad and parallel scan circuit input lines, and scan collector circuit connected between scan circuit output lines and another bond**

**pad**
Patent Assignee: WHETSEL L D (WHET-I); TEXAS INSTR INC ( **TEXI** )
Inventor: WHETSEL L D
Number of Countries: 001 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| US 20020196045 | A1 | 20021226 | US 2001836675 | A | 20010416 | 200375 B |
| | | | US 2001997540 | A | 20011129 | |
| US 6646460 | B2 | 20031111 | US 9764145 | P | 19971103 | 200382 |
| | | | US 98183885 | A | 19981030 | |
| | | | US 2001836675 | A | 20010416 | |
| | | | US 2001997540 | A | 20011129 | |

Priority Applications (No Type Date): US 2001836675 A 20010416; US 2001997540 A 20011129; US 9764145 P 19971103; US 98183885 A 19981030
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020196045 | A1 | | 17 | G01R-031/26 | Div ex application US 2001836675 |
| | | | | | Div ex patent US 6362015 |
| US 6646460 | B2 | | | G01R-031/02 | Provisional application US 9764145 |
| | | | | | Div ex application US 98183885 |
| | | | | | Div ex application US 2001836675 |
| | | | | | Div ex patent US 6242269 |
| | | | | | Div ex patent US 6362015 |

Abstract (Basic): US 20020196045 A1
NOVELTY - A **scan** distributor circuit (300) has a serial input connected to a bond pad (302) and has parallel outputs connected to input lines (304) of a parallel **scan** path circuit (324) which is formed on a substrate and connected to functional circuits. A collector circuit (344) has parallel inputs connected to output line (346) of the **scan** path circuit and a serial output connected to another bond pad (366).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for integrated circuit testing process.
USE - Integrated circuit having testing circuit with parallel **scan** path, **scan** distributor/collector circuits.
ADVANTAGE - Provides a way to amplify **test data input** to and output from an integrated circuit and to test complex core circuits embedded within integrated circuit by reuse of **scan** distributor/collector circuits at a low cost.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of parallel **scan** path test arrangement.
**scan** distributor circuit (300)
bond pads (302,366,370,434)
input lines of **scan** path circuit (304,322,372,390)
parallel **scan** path circuits (324,342,392,410)
parallel **scan** collector circuits (344,412)
output lines of **scan** path circuit (346,364,414,432)
pp; 17 DwgNo 3/12
Title Terms: INTEGRATE; CIRCUIT; **SCAN** ; DISTRIBUTE; CIRCUIT; CONNECT; ONE; BOND; PAD; PARALLEL; **SCAN** ; CIRCUIT; INPUT; LINE; **SCAN** ; COLLECT; CIRCUIT; CONNECT; **SCAN** ; CIRCUIT; OUTPUT; LINE; BOND; PAD
Derwent Class: S01; U11
International Patent Class (Main): G01R-031/02; G01R-031/26
File Segment: EPI

**29/5/3 (Item 3 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


015567145 **Image available**
WPI Acc No: 2003-629302/200360
XRPX Acc No: N03-500915

**Test access port for testing interconnect circuits, has clock input, data input and output, controller, instruction register, boundary scan register and delay circuit.**

Patent Assignee: TEXAS INSTR INC ( **TEXI** ) ; WHETSEL L D (WHET-I

Inventor: WHETSEL L D

Number of Countries: 035 Number of Patents: 005

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| EP 1335210 | A2 | 20030813 | EP 2003100257 | A | 20030207 | 200360 B |
| CN 1438492 | A | 20030827 | CN 2003104139 | A | 20030211 | 200375 |
| JP 2003344508 | A | 20031203 | JP 200372799 | A | 20030210 | 200381 |
| US 20030229835 | A1 | 20031211 | US 2002387043 | P | 20020610 | 200382 |
| | | | US 2003364100 | A | 20030211 | |
| KR 2003068052 | A | 20030819 | KR 20038324 | A | 20030210 | 200382 |

Priority Applications (No Type Date): US 2002387043 P 20020610; US 2002356582 P 20020211; US 2003364100 A 20030211

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 1335210 | A2 | E | 49 | G01R-031/3185 | |
| Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR | | | | | |
| CN 1438492 | A | | | G01R-031/28 | |
| JP 2003344508 | A | | 129 | G01R-031/28 | |
| US 20030229835 | A1 | | | G01R-031/28 | Provisional application US 2002387043 |
| KR 2003068052 | A | | | G01R-031/28 | |


Abstract (Basic): EP 1335210 A2

NOVELTY - The test access port includes a test clock input, a test mode select input, and **test data input** , and a **test data output** . There is also a controller connected to the test clock input and the mode select input. An instruction register is connected to the **test data input** and output. The boundary **scan** register is connected to functional data signals, the **test data input** and output, and the mode signal output.

DETAILED DESCRIPTION - The controller is used to provide an Update-DR signal, a clock DR signal, and update-DR signal, and a shift-DR signal. The controller has a control bus input. The instruction register has a control bus output connected to the controller, and has a mode signal output. The boundary **scan** register receives the Update-DR signal and the Shift-DR signal. The register also has a modified Clock-DR input. A delay circuit is connected to the test clock input, and provides a delayed clock output. Test circuitry is connected to the delayed clock output, the control bus, the Update-DR signal, the clock-DR signal, and the modified clock-DR input, to test the functional signals received by the boundary **scan** register. The test circuitry may comprise propagation test circuitry to test the propagation of the functional signals received by the boundary **scan** register. INDEPENDENT CLAIMS are included for a process or performing a test, and for a method of testing an interconnect circuit.

USE - For testing high speed AC and DC interconnect circuits located between integrated circuits.

ADVANTAGE - The apparatus provides for extending the JTAG instruction set and architecture, to provide a solution for testing of high speed integrated circuit to integrated circuit interconnect circuits.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic block diagram illustrating the improvement to the basic JTAG architecture

Boundary **scan** register (503)

TAP controller (601)

Instruction register (602)

Delay (603)

Bus (606)

pp; 49 DwgNo 6/30
Title Terms: TEST; ACCESS; PORT; TEST; INTERCONNECT; CIRCUIT; CLOCK; INPUT; DATA; INPUT; OUTPUT; CONTROL; INSTRUCTION; REGISTER; BOUNDARY; **SCAN** ; REGISTER; DELAY; CIRCUIT
Derwent Class: S01; T01; U11; V04
International Patent Class (Main): G01R-031/28; G01R-031/3185
International Patent Class (Additional): G06F-011/22
File Segment: EPI

**29/5/4 (Item 4 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014853663 **Image available**
WPI Acc No: 2002-674369/200272
XRPX Acc No: N02-533278
**Integrated NAND and flip-flip circuit for digital signal processor, includes pre-NAND scan circuit which produces output signals based on logical state of scan -enable signals, to NAND gate**
Patent Assignee: HILL A M (HILL-I); TEXAS INSTR INC ( **TEXI** )
Inventor: HILL A M
Number of Countries: 001 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020113624 | A1 | 20020822 | US 2000258679 | A | 20001227 | 200272 | B |
| | | | US 2001998823 | A | 20011203 | | |
| US 6492841 | B2 | 20021210 | US 2000258679 | A | 20001227 | 200301 | |
| | | | US 2001998823 | A | 20011203 | | |

Priority Applications (No Type Date): US 2000258679 P 20001227; US 2001998823 A 20011203
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020113624 | A1 | | 8 | H03K-019/20 | Provisional application US 2000258679 |
| US 6492841 | B2 | | | H03K-019/00 | Provisional application US 2000258679 |

Abstract (Basic): US 20020113624 A1
NOVELTY - A pre-NAND **scan** circuit (50) receives a pair of data signals (52,54), a **scan - in** signal (56) and a **scan** -enable signal (58). The pre-NAND circuit produces a pair of output signals (60,62) based on the received signals, such that the logical state of the output signals are set depending on the logical state of **scan** -enable signal. A NAND gate (48) receives the output signal from the pre-NAND circuit.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for flip-flop circuit.
USE - Integrated NAND and flip-flop circuit for digital signal processors that are used in cell phones, personal digital assistant, appliances, etc.
ADVANTAGE - As the pre-NAND circuit and the NAND gate perform the overall function, the number of logic gates required is reduced. Hence enhances the performance of the digital signal processors.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of integrated NAND and flip-flop circuit.
NAND gate (48)
Pre-NAND **scan** circuit (50)
Data signals (52,54)
**Scan - in** signal (56)
**Scan** -enable signal (58)
Output signals (60,62)
pp; 8 DwgNo 3/5
Title Terms: INTEGRATE; NAND; FLIP; FLIP; CIRCUIT; DIGITAL; SIGNAL; PROCESSOR; PRE; NAND; **SCAN** ; CIRCUIT; PRODUCE; OUTPUT; SIGNAL; BASED;

LOGIC; STATE; **SCAN** ; ENABLE; SIGNAL; NAND; GATE
Derwent Class: U13; U21; U22
International Patent Class (Main): H03K-019/00; H03K-019/20
File Segment: EPI

**29/5/5 (Item 5 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014649503 **Image available**
WPI Acc No: 2002-470207/200250
Related WPI Acc No: 1999-478614; 2000-374818; 2002-598507; 2005-056377
XRPX Acc No: N02-371134
**Integrated memory module has memory circuit having** switch **and bus holder circuit, is connected to input and output of output buffer at signal path, to detect and resolve voltage contention at the output terminal**
Patent Assignee: TEXAS INSTR INC ( **TEXI** )
Inventor: WHETSEL L D
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6378095 | B1 | 20020423 | US 99259186 | A | 19990226 | 200250 | B |
| | | | US 2000521319 | A | 20000309 | | |

Priority Applications (No Type Date): US 99259186 A 19990226; US 2000521319 A 20000309
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6378095 | B1 | | 29 | G01R-031/28 | Cont of application US 99259186<br>Cont of patent US 6055659 |

Abstract (Basic): US 6378095 B1
NOVELTY - A memory circuit has a feed back path connected to output and input terminal of an output buffer of a signal path. The memory circuit having a **switch** and a bus holder circuit, is selectively operable to detect and resolve voltage contention at the output terminal.
USE - Integrated memory module.
ADVANTAGE - The output buffer has the ability to establish safe **test data** at IC outputs when the IC is **switched** from functional mode to boundary test mode. Quickly resolves voltage contention problems at IC output pins. Maintains stable **test data** at output pins while data is **captured** and shifted without using output hold memory.
DESCRIPTION OF DRAWING(S) - The figure shows the functional output memory block diagram.
pp; 29 DwgNo 12B/17
Title Terms: INTEGRATE; MEMORY; MODULE; MEMORY; CIRCUIT; **SWITCH** ; BUS; HOLD; CIRCUIT; CONNECT; INPUT; OUTPUT; OUTPUT; BUFFER; SIGNAL; PATH; DETECT; RESOLUTION; VOLTAGE; CONTENTION; OUTPUT; TERMINAL
Derwent Class: S01; U11; U13; U14
International Patent Class (Main): G01R-031/28
International Patent Class (Additional): H04L-001/22
File Segment: EPI

**29/5/6 (Item 6 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014261465 **Image available**
WPI Acc No: 2002-082163/200211
Related WPI Acc No: 2002-068187

XRPX Acc No: N02-061202
**Integrated circuit for boundary scan system, has boundary scan path that includes mixture of serially connected dedicated and shared boundary scan cells**
Patent Assignee: WHETSEL L D (WHET-I); TEXAS INSTR INC ( **TEXI** )
Inventor: WHETSEL L D
Number of Countries: 001 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| US 20010025356 | A1 | 20010927 | US 2000175181 | P | 20000110 | 200211 B |
| | | | US 2001758089 | A | 20010110 | |
| US 6728915 | B2 | 20040427 | US 2000175181 | P | 20000110 | 200429 |
| | | | US 2001758089 | A | 20010110 | |

Priority Applications (No Type Date): US 2000175181 P 20000110; US 2001758089 A 20010110
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20010025356 | A1 | | 12 | G01R-031/28 | Provisional application US 2000175181 |
| US 6728915 | B2 | | | G01R-031/28 | Provisional application US 2000175181 |

Abstract (Basic): US 20010025356 A1
NOVELTY - A boundary **scan** path includes a mixture of serially connected dedicated and shared boundary **scan** cells. A connection is formed between the **test data input** ( **TDI** ) terminal and boundary **scan** path input and another connection is formed between **test data output** ( **TDO** ) terminal and boundary **scan** path output.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Boundary **scan** test mode entering process;
(b) Intellectual property core circuit within an integrated circuit;
(c) Boundary **scan** system
USE - For boundary **scan** system (claimed).
ADVANTAGE - The dedicated **scan** cells of the **scan** path can be scanned without disturbing the functional mode of the circuit. As the shared **scan** cells use shared memories, the test circuitry overhead is reduced. The floating buses that cause high current situations are avoided.
DESCRIPTION OF DRAWING(S) - The figure shows the simplified block diagram of boundary **scan** path around a master integrated circuit and two slave integrated circuits.
**Test data input** ( **TDI** )
**Test data output** ( **TDO** )
pp; 12 DwgNo 6/9
Title Terms: INTEGRATE; CIRCUIT; BOUNDARY; **SCAN** ; SYSTEM; BOUNDARY; **SCAN** ; PATH; MIXTURE; SERIAL; CONNECT; DEDICATE; SHARE; BOUNDARY; **SCAN** ; CELL
Derwent Class: S01; U11
International Patent Class (Main): G01R-031/28
File Segment: EPI

**29/5/7 (Item 7 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014247487 **Image available**
WPI Acc No: 2002-068187/200210
Related WPI Acc No: 2002-082163
XRPX Acc No: N02-050492
**Integrated circuit with self boundary scan test function, has boundary scan paths having serially connected dedicated and shared boundary scan cells, connected between test data input and output terminals**
Patent Assignee: TEXAS INSTR INC ( **TEXI** ) ; WHETSEL L D (WHET-I

Inventor: WHETSEL L D
Number of Countries: 028 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| EP 1130409 | A2 | 20010905 | EP 2001200044 | A | 20010109 | 200210 B |
| JP 2001249168 | A | 20010914 | JP 20012712 | A | 20010110 | 200210 |
| US 20040187059 | A1 | 20040923 | US 2000175188 | P | 20000110 | 200463 |
| | | | US 2001758089 | A | 20010110 | |
| | | | US 2004814671 | A | 20040330 | |

Priority Applications (No Type Date): US 2000175188 P 20000110; US 2001758089 A 20010110; US 2004814671 A 20040330
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 1130409 | A2 | E | 12 | G01R-031/3185 | |
| Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR | | | | | |
| JP 2001249168 A | | | 8 | G01R-031/28 | |
| US 20040187059 A1 | | | | G01R-031/28 | Provisional application US 2000175188 |
| | | | | | Div ex application US 2001758089 |
| | | | | | Div ex patent US 6728915 |

Abstract (Basic): EP 1130409 A2
NOVELTY - Boundary **scan** paths (608,612) having serially connected **scan** cells (C) and shared boundary **scan** cells (D) are connected between **test data input** and output terminals ( **TDI** , **TDO** ). Multiplexers (636,638,640) are provided to selectively contacts dedicated or shared boundary **scan** cells between input and output terminals.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a process of entering into a boundary **scan** test mode.
USE - E.g. memory with self boundary **scan** test function.
ADVANTAGE - Secures safe entry into test mode from functional mode, as the dedicated **scan** cells can be accessed independent of the shared **scan** cells. Reduces circuitry overhead as the data **scan** cells use shared memories.
DESCRIPTION OF DRAWING(S) - The figure shows the block circuit diagram of IC.
Boundary **scan** paths (608,612)
Multiplexers (636,638,640)
Serially connected **scan** cells (C)
Shared boundary **scan** cells (D)
**Test data input** and output terminals (TD1, **TDO** )
pp; 12 DwgNo 6/9
Title Terms: INTEGRATE; CIRCUIT; SELF; BOUNDARY; **SCAN** ; TEST; FUNCTION; BOUNDARY; **SCAN** ; PATH; SERIAL; CONNECT; DEDICATE; SHARE; BOUNDARY; **SCAN** ; CELL; CONNECT; TEST; DATA; INPUT; OUTPUT; TERMINAL
Derwent Class: S01; U11
International Patent Class (Main): G01R-031/28; G01R-031/3185
International Patent Class (Additional): G06F-011/22
File Segment: EPI

**29/5/8 (Item 8 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014139845 **Image available**
WPI Acc No: 2001-624056/200172
Related WPI Acc No: 1997-558436; 2000-085840; 2002-147116; 2004-674581
XRPX Acc No: N01-464880
**Boundary** scan **input/output serializer circuit for inputting test patterns to and outputting test patterns from circuits during a single data register** scan **operation**

Patent Assignee: TEXAS INSTR INC ( **TEXI** )
Inventor: WHETSEL L D
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6189115 | B1 | 20010213 | US 93101503 | A | 19930730 | 200172 | B |
| | | | US 95391291 | A | 19950221 | | |
| | | | US 97885464 | A | 19970627 | | |
| | | | US 99430932 | A | 19991101 | | |

Priority Applications (No Type Date): US 93101503 A 19930730; US 95391291 A 19950221; US 97885464 A 19970627; US 99430932 A 19991101
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6189115 | B1 | | 41 | G06F-011/13 | Cont of application US 93101503<br>Cont of application US 95391291<br>Div ex application US 97885464<br>Cont of patent US 5687312<br>Div ex patent US 6006343 |

Abstract (Basic): US 6189115 B1

NOVELTY - A boundary input/output serializer receives input from a **test data input** pin (102) and control buses (108,110) and outputs control to data registers (DREG 1,2) via a control bus (126) and serial data to a **test data output** pin (116) via multiplexers (MUX 1,2). The serializer is selected to transfer data from the input to the output and, when the serializer is disabled, a connection is made between the input and output, to allow the registers to be accessed directly by the test access port (TAP).

USE - Serial testing of electrical circuits via **scan** access.

ADVANTAGE - More efficient testing.

DESCRIPTION OF DRAWING(S) - The drawing is a block diagram of the serial **scan** test architecture according to the invention

**Test data input** and output pins (102,116)

Control buses (108,110)

Data registers (DREG 1,2)

Test access port (TAP)

pp; 41 DwgNo 8/29

Title Terms: BOUNDARY; **SCAN** ; INPUT; OUTPUT; CIRCUIT; INPUT; TEST; PATTERN ; OUTPUT; TEST; PATTERN; CIRCUIT; SINGLE; DATA; REGISTER; **SCAN** ; OPERATE
Derwent Class: S01; T01; U11; U21; V04
International Patent Class (Main): G06F-011/13
File Segment: EPI

**29/5/9 (Item 9 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


013202945 **Image available**
WPI Acc No: 2000-374818/200032
Related WPI Acc No: 1999-478614; 2002-470207; 2002-598507; 2005-056377
XRPX Acc No: N00-281405

**Memory circuitry of boundary scan design based integrated circuit, has switch and output buffer connected in series between memory and output terminals, and input buffer is connected in parallel to output buffer**

Patent Assignee: TEXAS INSTR INC ( **TEXI** )
Inventor: WHETSEL L D
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6055659 | A | 20000425 | US 99259186 | A | 19990226 | 200032 | B |

Priority Applications (No Type Date): US 99259186 A 19990226
Patent Details:

Patent No  Kind Lan Pg  Main IPC  Filing Notes
US 6055659  A  29 G01R-031/28

Abstract (Basic): US 6055659 A

NOVELTY - The buffer circuit comprises a **switch** and output buffer connected in series in between memory and output terminals of integrated circuit. An input buffer electrically weaker than output buffer is connected in parallel to the input terminal. The input and output buffers constitute a latch circuit.

DETAILED DESCRIPTION - The integrated circuit comprises a functional circuit, an output terminal, a **test data** path and a memory. The memory is selectively connected to functional circuits and **test data** path through a test control circuit. The **switch** in the buffer circuit is a three state buffer **switch** .

USE - For boundary scan design based integrated circuit used in computer systems.

ADVANTAGE - Establishes safe **test data** at IC output when IC is **switched** from functional mode to boundary test mode. Solves voltage output problems at IC output pins due to short circuit between pins, ground or supply voltage. Maintains stable **test data** at output pins without need for output hold memory, when the data is **captured** and shifted through shared **capture** /shift memories.

DESCRIPTION OF DRAWING(S) - The figure shows circuit diagram of boundary scan design for two state output IC.

pp; 29 DwgNo 7/17

Title Terms: MEMORY; CIRCUIT; BOUNDARY; SCAN; DESIGN; BASED; INTEGRATE; CIRCUIT; **SWITCH** ; OUTPUT; BUFFER; CONNECT; SERIES; MEMORY; OUTPUT; TERMINAL; INPUT; BUFFER; CONNECT; PARALLEL; OUTPUT; BUFFER
Derwent Class: S01; U11; U14
International Patent Class (Main): G01R-031/28
File Segment: EPI

**29/5/10 (Item 10 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


012588623 **Image available**
WPI Acc No: 1999-394730/199933
XRPX Acc No: N99-295052
**Integrated testing circuit in integrated circuit (IC) memory device**
Patent Assignee: TEXAS INSTR INC ( **TEXI** )
Inventor: DORNEY T D
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| US 5920573 | A | 19990706 | US 9620369 | A | 19960625 | 199933 B |
| | | | US 96681190 | A | 19960722 | |

Priority Applications (No Type Date): US 9620369 P 19960625; US 96681190 A 19960722
Patent Details:
Patent No  Kind Lan Pg  Main IPC  Filing Notes
US 5920573  A  23 G11C-029/00  Provisional application US 9620369

Abstract (Basic): US 5920573 A

NOVELTY - **Multiplexers** (230,232,234,236,238,240), each associated with two different arrays of cells, combine the inputs from the associated cell arrays whose outputs are fed to comparators (242,244,246,250). On reception of **test data** bits from arrays (32-46) of addressable cells, the potential state on each quadrant common line is changed when any comparison fails.

DETAILED DESCRIPTION - The addressable storage cells are formed into arrays which form quadrants. A **test data** bit is applied through a pin to the storage cells from a writing circuit. An expected

data bit is received by a circuit. The stored test data bit in each of the storage cells is read by a read-out circuit. Based on the potential state on all the four common lines, a transmission circuit transmits the potential states of the read-out data from the storage cells. The comparator circuits are placed in close proximity to multiplier circuits which are placed in close proximity to the storage cells. Separate input/output pins are provided for carrying the input and output data bits. In **response** to a column address change in a quadrant, a column line circuit establishes a potential state on each quadrant-specific common line. An INDEPENDENT CLAIM is also included for an IC testing method in memory devices.

USE - For use in an IC memory device and in some application specific memory devices where additional control signals may be used.

ADVANTAGE - Single internal read and write line can be used for each quadrant to perform read write operations. The read operation performed by the circuit uses only four quadrant-specific common lines which allow the x4 laser repair test to be implemented. The static pull up transistor is replaced by a dynamic transistor for implementing low voltage in the common line.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of one quadrant of the integrated testing circuit.

arrays (32-46)

**multiplexers** (230,232,234,236,238,240)

comparators (242,244,246,250)

pp; 23 DwgNo 5/26

Title Terms: INTEGRATE; TEST; CIRCUIT; INTEGRATE; CIRCUIT; IC; MEMORY; DEVICE

Derwent Class: S01; U11; U14

International Patent Class (Main): G11C-029/00

File Segment: EPI

**29/5/11 (Item 11 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



012081116 **Image available**

WPI Acc No: 1998-498027/199843

Related WPI Acc No: 2004-489902

XRPX Acc No: N98-389046

**Probeless testing of integrated circuit on semiconductor wafer - using switches located in test paths between output buffer and tester, and voltmeter to measure output response of buffer**

Patent Assignee: TEXAS INSTR INC ( TEXI ) ; WHETSEL L D (WHET-I

Inventor: WHETSEL L D

Number of Countries: 028 Number of Patents: 010

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 867727 | A2 | 19980930 | EP 98200962 | A | 19980326 | 199843 | B |
| JP 11030652 | A | 19990202 | JP 9881972 | A | 19980327 | 199915 | |
| KR 98080795 | A | 19981125 | KR 9810773 | A | 19980327 | 200005 | |
| US 6199182 | B1 | 20010306 | US 9741729 | P | 19970327 | 200115 | |
| | | | US 9849626 | A | 19980327 | | |
| TW 421845 | A | 20010211 | TW 98104590 | A | 19980407 | 200146 | |
| US 20010014959 | A1 | 20010816 | US 9741729 | P | 19970327 | 200149 | |
| | | | US 9849626 | A | 19980327 | | |
| | | | US 2000745523 | A | 20001221 | | |
| US 6731106 | B2 | 20040504 | US 9741729 | P | 19970327 | 200430 | |
| | | | US 9849626 | A | 19980327 | | |
| | | | US 2000745523 | A | 20001221 | | |
| EP 867727 | B1 | 20040602 | EP 98200962 | A | 19980326 | 200441 | |
| | | | EP 2004100986 | A | 19980326 | | |
| DE 69824226 | E | 20040708 | DE 98624226 | A | 19980326 | 200445 | |
| | | | EP 98200962 | A | 19980326 | | |
| US 20040181729 | A1 | 20040916 | US 9741729 | P | 19970327 | 200461 | |

| | | |
|---|---|---|
| US 9849626 | A | 19980327 |
| US 2000745523 | A | 20001221 |
| US 2004806539 | A | 20040323 |

Priority Applications (No Type Date): US 9741729 P 19970327; US 9741619 P 19970327; US 9741621 P 19970327; US 9849626 A 19980327; US 2000745523 A 20001221; US 2004806539 A 20040323
Cited Patents: No-SR.Pub
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 867727 | A2 | E | 41 | G01R-031/265 | |
| Designated States (Regional): AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI | | | | | |
| JP 11030652 | A | | 30 | G01R-031/28 | |
| KR 98080795 | A | | | G01R-031/26 | |
| US 6199182 | B1 | | | G01R-031/28 | Provisional application US 9741729 |
| TW 421845 | A | | | H01L-021/66 | |
| US 20010014959 | A1 | | | G01R-031/28 | Provisional application US 9741729<br>Div ex application US 9849626<br>Div ex patent US 6199182 |
| US 6731106 | B2 | | | G01R-031/28 | Provisional application US 9741729<br>Div ex application US 9849626<br>Div ex patent US 6199182 |
| EP 867727 | B1 | E | | G01R-031/265 | Related to application EP 2004100986 |
| Designated States (Regional): DE FR GB IT NL | | | | | |
| DE 69824226 | E | | | G01R-031/265 | Based on patent EP 867727 |
| US 20040181729 | A1 | | | G01R-031/28 | Provisional application US 9741729<br>Div ex application US 9849626<br>Div ex application US 2000745523<br>Div ex patent US 6199182<br>Div ex patent US 6731106 |

Abstract (Basic): EP 867727 A

The method is for testing the output circuitry of an integrated circuit, which includes an output buffer (350) having an input coupled to core functional circuitry and an output coupled to a terminal pad. The method comprises disconnecting the input of the output buffer from the core functional circuitry, and connecting the input and output of the output buffer to a first and a second test terminal, respectively.

A **test signal** is applied at a first logic level to the first test terminal, for receipt by output buffer, and the drive strength of the output buffer in **response** to the **test signal** is measured at the second test terminal. A second **test signal** at a second logic level is applied to the first test terminal, for receipt by output buffer, and the drive strength of the output buffer in **response** to the **test signal** at the second logic level is then measured at the second test terminal. The output buffer output is connected to load test terminal, with load connected prior to applying **test signals** . Drive strength of the output buffer may be measured by measuring voltage drop across the load to determine drive current from the output buffer.

ADVANTAGE - Eliminates heat build-up after circuit has been tested.

Dwg.37/42

Title Terms: TEST; INTEGRATE; CIRCUIT; SEMICONDUCTOR; WAFER; **SWITCH** ; LOCATE; TEST; PATH; OUTPUT; BUFFER; TEST; VOLTMETER; MEASURE; OUTPUT; RESPOND; BUFFER
Derwent Class: S01; T01; U21
International Patent Class (Main): G01R-031/26; G01R-031/265; G01R-031/28; H01L-021/66
International Patent Class (Additional): G01R-031/3185; G06F-011/00; G06F-011/267
File Segment: EPI

29/5/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX


011799888 **Image available**
WPI Acc No: 1998-216798/199819
Related WPI Acc No: 1998-130116
XRPX Acc No: N98-171420
**Self-initialising and correcting shared resource boundary** scan **with output latching - includes output buffer structure which** is responsive to **initiation of test mode for latching, at output terminal, functional** test data **from shared** capture **-shift memory to resolve voltage contention at output terminal**
Patent Assignee: TEXAS INSTR INC ( **TEXI** )
Inventor: WHETSEL L D
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5732091 | A | 19980324 | US 94342525 | A | 19941121 | 199819 | B |
| | | | US 96690379 | A | 19960730 | | |
| | | | US 97783185 | A | 19970115 | | |

Priority Applications (No Type Date): US 94342525 A 19941121; US 96690379 A 19960730; US 97783185 A 19970115
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5732091 | A | | 15 | G01R-031/28 | Cont of application US 94342525 |
| | | | | | Cont of application US 96690379 |

Abstract (Basic): US 5732091 A
An output boundary **scan** cell includes an output buffer structure (51) connected between a shared **capture** -shift memory (17) and an output terminal. The output buffer structure is responsive to initiation of a test mode of operation for latching at the output terminal functional **test data** from the shared **capture** /shift memory, and is operable to resolve voltage contention at the output terminal.
ADVANTAGE - Establishes safe **test data** at IC outputs when IC is **switched** from functional mode to boundary test mode without first having to **scan** safe **test data in** . Quickly resolves voltage contention problems at IC output pins due to shorts between pins, ground or supply voltage. Maintains stable **test data** at output pins while data is **captured** and shifted through shared **capture** -shift memories, without having to use output hold memory.
Dwg.7/10
Title Terms: SELF; INITIALISE; CORRECT; SHARE; RESOURCE; BOUNDARY; **SCAN** ; OUTPUT; LATCH; OUTPUT; BUFFER; STRUCTURE; RESPOND; INITIATE; TEST; MODE; LATCH; OUTPUT; TERMINAL; FUNCTION; TEST; DATA; SHARE; **CAPTURE** ; SHIFT; MEMORY; RESOLUTION; VOLTAGE; CONTENTION; OUTPUT; TERMINAL
Derwent Class: S01; T01
International Patent Class (Main): G01R-031/28
File Segment: EPI

29/5/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX


011713206 **Image available**
WPI Acc No: 1998-130116/199812
Related WPI Acc No: 1998-216798
XRPX Acc No: N98-102760
**IC with boundary** scan **cell memories for testing - includes signal path between functional logic and terminal including buffer with feedback path**

**connected from buffer output to its input**
Patent Assignee: TEXAS INSTR INC ( **TEXI** )
Inventor: WHETSEL L D
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| US 5715255 | A | 19980203 | US 94342525 | A | 19941121 | 199812 B |
| | | | US 95431156 | A | 19950428 | |
| | | | US 96769971 | A | 19961219 | |

Priority Applications (No Type Date): US 95431156 A 19950428; US 94342525 A 19941121; US 96769971 A 19961219
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5715255 | A | | 30 | G06F-011/00 | CIP of application US 94342525<br>Cont of application US 95431156 |

Abstract (Basic): US 5715255 A
The integrated circuit includes logic performing logic functions of the integrated circuit. An output terminal is accessible externally of the integrated circuit. A signal path connected between the functional logic and the terminal carries signals between them. The signal path includes a buffer having an output connected to one of the terminal and the functional logic. The signal path also includes a memory element including the buffer and a switch connected to an input of the buffer.
The output of the buffer is connected to the output terminal. A feedback path is connected to the buffer output and to a buffer input for carrying feedback signals from the output to the input.
ADVANTAGE - Eliminates need for high-drive buffers between FIMs and FCL. Provides FOM structure which can resolve voltage contention at output pin, reduce signal path delays associated with conventional FIM and FOM structures and their combinations in boundary **scan** cells. Provides boundary **scan** operation without speed penalty to function operation. Can establish safe test data at IC outputs when switched from functional to boundary test mode without having to **scan** safe **test data in** .
Dwg.8/17
Title Terms: IC; BOUNDARY; **SCAN** ; CELL; MEMORY; TEST; SIGNAL; PATH; FUNCTION; LOGIC; TERMINAL; BUFFER; FEEDBACK; PATH; CONNECT; BUFFER; OUTPUT; INPUT
Index Terms/Additional Words: FUNCTIONAL; INPUT; MEMORY; FUNCTIONAL; CORE; LOGIC; FUNCTIONAL; OUTPUT; MEMORY
Derwent Class: T01
International Patent Class (Main): G06F-011/00
File Segment: EPI

**29/5/14 (Item 14 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


011035973 **Image available**
WPI Acc No: 1997-013897/199702
XRPX Acc No: N97-012069
**Boundary scan cell for integrated circuit input and output pin - has transmission gates to** switch **test voltage to path carrying analog signal with test voltage maintained**
Patent Assignee: TEXAS INSTR INC ( **TEXI** )
Inventor: WHETSEL L D
Number of Countries: 007 Number of Patents: 005
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| EP 745935 | A1 | 19961204 | EP 96303954 | A | 19960531 | 199702 B |
| JP 9218249 | A | 19970819 | JP 96138638 | A | 19960531 | 199743 |
| US 5872908 | A | 19990216 | US 95454795 | A | 19950531 | 199914 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | US 97784432 | A | 19970116 | |
| EP 745935 | B1 | 20031119 | EP 96303954 | A | 19960531 | 200377 |
| DE 69630730 | E | 20031224 | DE 630730 | A | 19960531 | 200408 |
| | | | EP 96303954 | A | 19960531 | |

Priority Applications (No Type Date): US 95454795 A 19950531; US 97784432 A 19970116
Cited Patents: 4.Jnl.Ref
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 745935 | A1 | E | 28 | G06F-011/22 | |
| Designated States (Regional): DE FR GB IT NL | | | | | |
| JP 9218249 | A | | 22 | G01R-031/28 | |
| US 5872908 | A | | | H04B-017/00 | Cont of application US 95454795 |
| EP 745935 | B1 | E | | G06F-011/22 | |
| Designated States (Regional): DE FR GB IT NL | | | | | |
| DE 69630730 | E | | | G06F-011/22 | Based on patent EP 745935 |

Abstract (Basic): EP 745935 A

The boundary scan cell logic includes an input **multiplexer** ( **MUX1** ), a **capture** /shift memory (MEM1), two transmission gates (TG1,TG2) and a latch buffer. The output memory function is realised by the combination of the IC output buffer, the latch buffer and the second transmission gate. The two transmission gates realise the output memory function and this with the IC core logic shares use of the IC output buffer.

A signal path carries an analog signal to which a test voltage is applied and is maintained on the signal path independently of the test voltage node. In normal operation system data is passed to the output buffer via the first gate with the other disabled. In the test mode the second gate passes **test data** from MEM1 to the input of a latchable output buffer (40) with the first gate disabled.

ADVANTAGE - Simplifies testing of IC along with its wiring interconnection. Boundary scan cell requires less logic in IC core region and uses respective input and output IC buffers as part of input and output boundary scan cells. Provides boundary scan cell and output buffer combination that can immediately and asynchronously detect and correct short circuit conditions on output pins during Extest operation or when IC is being powered up in normal mode.

Dwg.4/22

Title Terms: BOUNDARY; SCAN; CELL; INTEGRATE; CIRCUIT; INPUT; OUTPUT; PIN; TRANSMISSION; GATE; **SWITCH** ; TEST; VOLTAGE; PATH; CARRY; ANALOGUE; SIGNAL; TEST; VOLTAGE; MAINTAIN
Derwent Class: S01; T01; U11; U13
International Patent Class (Main): G01R-031/28; G06F-011/22; H04B-017/00
International Patent Class (Additional): G01R-031/3167; H01L-021/822; H01L-027/04
File Segment: EPI

**29/5/15 (Item 15 from file: 350)**



010782741 **Image available**
WPI Acc No: 1996-279694/199629
XRPX Acc No: N96-235170

**Boundary scan-cells at input and output of integrated circuits - simplifies testing wiring interconnections by asynchronously detecting-correcting output short-circuit conditions when initially powering-up**

Patent Assignee: TEXAS INSTR INC ( **TEXI** ) ; WHETSEL L D (WHET-I
Inventor: WHETSEL L D
Number of Countries: 007 Number of Patents: 010
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| EP 717287 | A2 | 19960619 | EP 95309149 | A | 19951215 | 199629 B |
| JP 8233908 | A | 19960913 | JP 95327653 | A | 19951215 | 199647 |
| EP 717287 | A3 | 19961127 | EP 95309149 | A | 19951215 | 199702 |
| US 5701307 | A | 19971223 | US 94357476 | A | 19941216 | 199806 |
| | | | US 96711137 | A | 19960909 | |
| US 5847561 | A | 19981208 | US 94358128 | A | 19941216 | 199905 |
| | | | US 95509405 | A | 19950731 | |
| | | | US 97839532 | A | 19970414 | |
| US 5859860 | A | 19990112 | US 94357476 | A | 19941216 | 199910 |
| | | | US 96711137 | A | 19960909 | |
| | | | US 97910536 | A | 19970724 | |
| US 6694465 | B1 | 20040217 | US 94357476 | A | 19941216 | 200413 |
| | | | US 96711137 | A | 19960909 | |
| | | | US 97910536 | A | 19970724 | |
| | | | US 97949429 | A | 19971014 | |
| | | | US 99154381 | A | 19990916 | |
| | | | US 2000686709 | A | 20001011 | |
| US 20040163022 | A1 | 20040819 | US 94357476 | A | 19941216 | 200455 |
| | | | US 96711137 | A | 19960909 | |
| | | | US 97910536 | A | 19970724 | |
| | | | US 97949429 | A | 19971014 | |
| | | | US 98154381 | A | 19980916 | |
| | | | US 2000686709 | A | 20001011 | |
| | | | US 2004773784 | A | 20040206 | |
| EP 717287 | B1 | 20041013 | EP 95309149 | A | 19951215 | 200467 |
| DE 69533640 | E | 20041118 | DE 95633640 | A | 19951215 | 200476 |
| | | | EP 95309149 | A | 19951215 | |

Priority Applications (No Type Date): US 95509405 A 19950731; US 94357476 A 19941216; US 94358128 A 19941216; US 96711137 A 19960909; US 97839532 A 19970414; US 97910536 A 19970724; US 97949429 A 19971014; US 99154381 A 19990916; US 2000686709 A 20001011; US 98154381 A 19980916; US 2004773784 A 20040206

Cited Patents: No-SR.Pub; 2.Jnl.Ref; EP 522413; GB 2266965; US 5134314

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 717287 | A2 | E | 30 | G01R-031/3185 | |
| Designated States (Regional): DE FR GB IT NL | | | | | |
| JP 8233908 | A | | 26 | G01R-031/28 | |
| EP 717287 | A3 | | | G01R-031/3185 | |
| US 5701307 | A | | 18 | G01R-031/28 | Cont of application US 94357476 |
| US 5847561 | A | | | G01R-031/28 | CIP of application US 94358128 |
| | | | | | Cont of application US 95509405 |
| US 5859860 | A | | | G06F-011/00 | Cont of application US 94357476 |
| | | | | | Cont of application US 96711137 |
| | | | | | Cont of patent US 5701307 |
| US 6694465 | B1 | | | G01R-031/28 | Cont of application US 94357476 |
| | | | | | Cont of application US 96711137 |
| | | | | | Cont of application US 97910536 |
| | | | | | Cont of application US 97949429 |
| | | | | | Div ex application US 99154381 |
| | | | | | Cont of patent US 5701307 |
| | | | | | Cont of patent US 5859860 |
| US 20040163022 | A1 | | | G01R-031/28 | Cont of application US 94357476 |
| | | | | | Cont of application US 96711137 |
| | | | | | Cont of application US 97910536 |
| | | | | | Cont of application US 97949429 |
| | | | | | Div ex application US 98154381 |
| | | | | | Div ex application US 2000686709 |
| | | | | | Cont of patent US 5701307 |
| | | | | | Cont of patent US 5859860 |
| | | | | | Div ex patent US 6694465 |
| EP 717287 | B1 | E | | G01R-031/3185 | |

Designated States (Regional): DE FR GB IT NL
DE 69533640 E G01R-031/3185 Based on patent EP 717287

Abstract (Basic): EP 717287 A

The method operates an integrated circuit (IC) contg. normal functional and output circuitry for driving signals to the IC output terminals. The output circuits are disconnected from the functional circuitry for initial powering-up. Then a **test signal**, including scanning **test data**, is input to the output circuits, and the expected **response** observed for occurrence at the output terminals.

A disable signal opens a **switch** (TG1) between the functional and output circuitry, and also sets a drive strength level less than the full drive level. Any output terminal voltage contention is resolved, and any short-circuit thereat repaired, before the functional circuitry is re-connected.

USE/ADVANTAGE - Integrated circuit boundary scan testing, for allowing power-up and preventing latchable output buffer (40) from short-circuit damage/destruction, with increased scan-cell functionality and reduced logic overhead.

Dwg.4/27

Title Terms: BOUNDARY; SCAN; CELL; INPUT; OUTPUT; INTEGRATE; CIRCUIT; SIMPLIFY; TEST; WIRE; INTERCONNECT; ASYNCHRONOUS; DETECT; CORRECT; OUTPUT; SHORT; CIRCUIT; CONDITION; INITIAL; POWER; UP
Derwent Class: S01; U11
International Patent Class (Main): G01R-031/28; G01R-031/3185; G06F-011/00
International Patent Class (Additional): G06F-011/22; G06F-011/267; H01L-021/82
File Segment: EPI

**29/5/16 (Item 16 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


009910251 **Image available**
WPI Acc No: 1994-177957/199422
XRPX Acc No: N94-140169

**Comparator circuit for IC testing system - has device tester linked to DUT with data coupled via comparator giving one signal for tester analysis from comparison of four DUT outputs**

Patent Assignee: TEXAS INSTR INC ( **TEXI** )
Inventor: HII F; ROUSEY J E; SINGH I
Number of Countries: 001 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 600655 | A2 | 19940608 | EP 93309308 | A | 19931123 | 199422 | B |
| US 5422892 | A | 19950606 | US 92979994 | A | 19921123 | 199528 | |
| | | | US 94284911 | A | 19940802 | | |
| EP 600655 | A3 | 19961211 | EP 93309308 | A | 19931123 | 199707 | |

Priority Applications (No Type Date): US 92979994 A 19921123; US 94284911 A 19940802
Cited Patents: No-SR.Pub; EP 206486; US 4768194; US 4916700
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 600655 | A2 | E | 6 | G11C-029/00 | |
| US 5422892 | A | | 5 | G01R-031/28 | Cont of application US 92979994 |
| EP 600655 | A3 | | | G11C-029/00 | |

Abstract (Basic): EP 600655 A

The integrated circuit testing system includes a device tester (30) connected with the device-under-test (DUT)(31) and a comparator circuit (91). The device tester has address and control lines (32-34,36) connected to the DUT. The data line (45) and write enable line (35) pass via the comparator to the DUT.

When supplying write data to the DUT, the comparator has multiple output lines (37-40) to duplicate the tester output. The write enable line operates four **switches** (80-83) to effect this. When data is received from the DUT, these outputs are compared with each other in the comparator to give one signal for the tester.

ADVANTAGE - Allows tester to use only one transceiver circuit to test multiple memory paths in one DUT.

Dwg.1/1

Title Terms: COMPARATOR; CIRCUIT; IC; TEST; SYSTEM; DEVICE; TEST; LINK; DATA; COUPLE; COMPARATOR; ONE; SIGNAL; TEST; ANALYSE; COMPARE; FOUR; OUTPUT

Derwent Class: U11; U14

International Patent Class (Main): G01R-031/28; G11C-029/00

File Segment: EPI

29/5/17 **(Item 17 from file: 350)**



008828611 **Image available**

WPI Acc No: 1991-332628/199145

XRPX Acc No: N91-254936

**Power supply for semiconductor test system - supplies programmed** test pattern **voltages and** switches **current range resistors without effecting output voltage**

Patent Assignee: TEXAS INSTR INC ( **TEXI** )

Inventor: HEATON D A

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5059889 | A | 19911022 | US 90490803 | A | 19900308 | 199145 | B |

Priority Applications (No Type Date): US 90490803 A 19900308

Abstract (Basic): US 5059889 A

The device power supply in a semiconductor test system supplies programmed voltages to a semiconductor device under test and for current range **switching** of a current range impedance without affecting the output voltage of the device power supply. A closed loop voltage feedback circuit maintains at the device under test the programmed voltage. A closed loop current feedback circuit has its input across the current range impedance. The current feedback circuit functions independent of the closed loop voltage feedback circuit. A number of current range **switches** are connected inside the closed loop voltage feedback circuit. A compensation capacitor has its value programmed to optimise frequency **response** at the output circuit baseed on the capacitive load at the output.

The device power supply circuit operates in an auto-crossover servo loop, allowing the power supply to be programmed as a voltage source and a current source at the same time. Functions as a voltage source as long as a programmed current limit is not exceeded.

USE/ADVANTAGE - For VSLI test system and parametric measurement unit in semiconductor test equipment. Implements current range **switching** without effecting output voltage of OPS.

Dwg.1/3

Title Terms: POWER; SUPPLY; SEMICONDUCTOR; TEST; SYSTEM; SUPPLY; PROGRAM; TEST; PATTERN; VOLTAGE; **SWITCH** ; CURRENT; RANGE; RESISTOR; EFFECT; OUTPUT; VOLTAGE

Index Terms/Additional Words: PARAMETER; MEASURE; UNIT

Derwent Class: S01; U11; U24

International Patent Class (Additional): H02M-003/33

File Segment: EPI

**29/5/18 (Item 18 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


008815387 **Image available**
WPI Acc No: 1991-319400/199144
XRPX Acc No: N91-244846
Scan **path testing for multiple frequency circuits - disabling multiple system clocks using controller and using master clock to drive each module**
Patent Assignee: TEXAS INSTR INC ( **TEXI** )
Inventor: SRIDHAR T
Number of Countries: 008 Number of Patents: 007
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 454320 | A | 19911030 | EP 91303174 | A | 19910410 | 199144 | B |
| CN 1056003 | A | 19911106 | CN 91102504 | A | 19910418 | 199232 | |
| CN 1026727 | C | 19941123 | CN 91102504 | A | 19910418 | 199546 | |
| EP 454320 | B1 | 19951213 | EP 91303174 | A | 19910410 | 199603 | |
| DE 69115338 | E | 19960125 | DE 615338 | A | 19910410 | 199609 | |
| | | | EP 91303174 | A | 19910410 | | |
| US 5488613 | A | 19960130 | US 90511677 | A | 19900420 | 199611 | |
| | | | US 92988383 | A | 19921208 | | |
| KR 220001 | B1 | 19990901 | KR 916305 | A | 19910419 | 200104 | |

Priority Applications (No Type Date): US 90511677 A 19900420; US 92988383 A 19921208
Cited Patents: EP 108255; EP 108256
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 454320 | A | | | | |
| Designated States (Regional): DE FR GB IT NL | | | | | |
| CN 1056003 | A | | | G01R-031/28 | |
| CN 1026727 | C | | | G01R-031/28 | |
| EP 454320 | B1 | E | 9 | G06F-011/26 | |
| Designated States (Regional): DE FR GB IT NL | | | | | |
| DE 69115338 | E | | | G06F-011/26 | Based on patent EP 454320 |
| US 5488613 | A | | 5 | G01R-031/28 | Cont of application US 90511677 |
| KR 220001 | B1 | | | G01R-031/28 | |

Abstract (Basic): EP 454320 A
The method involves using a circuit (8) which contains three circuit modules (10a-c). Each module is controlled by its own clock (CKLK1, CLK2, CLK3) during normal operation of the circuit. The modules communicate over connections (12a,12b),. Multiplexers (14a-c) connect either these clocks or a master clock (MCLK) to the circuits as defined by a signal from the test system. A test data controller (16) is connected to the **scan** path through the modules. During testing, test data is shifted into ( **TDI** ) the modules and the module output is collected ( **TDO** ) for checking.
USE/ADVANTAGE - Avoids partitioning problems and delays in such circuits.
Dwg.2/2
Title Terms: **SCAN** ; PATH; TEST; MULTIPLE; FREQUENCY; CIRCUIT; DISABLE; MULTIPLE; SYSTEM; CLOCK; CONTROL; MASTER; CLOCK; DRIVE; MODULE
Derwent Class: S01; U11; U13
International Patent Class (Main): G01R-031/28; G06F-011/26
International Patent Class (Additional): G01R-031/28; AFG0-6F011/26
File Segment: EPI

**29/5/19 (Item 19 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


008490872 **Image available**

WPI Acc No: 1990-377872/199051
XRPX Acc No: N90-287989
**Line interface circuit facilitating testing - generates test signal of amplitude not crossing threshold level for allowing to maintain connection of input-output units during testing**
Patent Assignee: TEXAS INSTR INC ( **TEXI** ) ; TEXAS INSTR LTD ( **TEXI** )
Inventor: FATTORI F R; KERSLAKE R M
Number of Countries: 007 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 403147 | A | 19901219 | EP 90306136 | A | 19900606 | 199051 | B |
| JP 3129949 | A | 19910603 | JP 8913952 | A | 19890616 | 199128 | |
| US 5128962 | A | 19920707 | US 90523784 | A | 19900515 | 199230 | |
| EP 403147 | A3 | 19920826 | EP 90306136 | A | 19900606 | 199337 | |
| EP 403147 | B1 | 19970108 | EP 90306136 | A | 19900606 | 199707 | |
| DE 69029606 | E | 19970220 | DE 629606 | A | 19900606 | 199713 | |
| | | | EP 90306136 | A | 19900606 | | |

Priority Applications (No Type Date): GB 8913952 A 19890616
Cited Patents: NoSR.Pub; 3.Jnl.Ref; EP 176646; JP 11026841; JP 60020664; JP 61231646
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5128962 | A | | 9 | H04B-003/46 | |
| EP 403147 | B1 | E | 17 | H04L-001/24 | |
| Designated States (Regional): DE FR GB IT NL | | | | | |
| DE 69029606 | E | | | H04L-001/24 | Based on patent EP 403147 |

Abstract (Basic): EP 403147 A
The interface circuit has an output unit for feeding an output signal to a first conductor of the line. The output signal has parts with a steady level above a threshold range of levels and parts with a steady level below the threshold range of levels. An input unit receives an input signal from a second conductor of the line, and a device selectively applies a signal from the output unit directly to the input unit without traversing the line to enable the circuit to be tested. The output unit includes a device for selectively producing a **test signal** on a steady level of the output signal. The **test signal** is of such limited amplitude that it does not cross the threshold level so that during a test it is not necessary to disconnect the output unit from the line. The input unit includes a device responsive to the **test signal** to provide an indication of the functioning of the circuit. The output init includes a clamping device which is effective when the **test signal** is to be produced to limit the voltage so that it does not cross the threshold level.
ADVANTAGE - Elimination of need for **switches** between interface and line. (10pp Dwg.No.2/5)
Title Terms: LINE; INTERFACE; CIRCUIT; FACILITATE; TEST; GENERATE; TEST; SIGNAL; AMPLITUDE; CROSS; THRESHOLD; LEVEL; ALLOW; MAINTAIN; CONNECT; INPUT; OUTPUT; UNIT; TEST
Derwent Class: W01; W02
International Patent Class (Main): H04B-003/46; H04L-001/24
International Patent Class (Additional): H04B-017/00; H04L-025/02; H04L-029/14
File Segment: EPI

**29/5/20 (Item 20 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


008115228 **Image available**
WPI Acc No: 1990-002229/199001
XRPX Acc No: N90-001608
**Testable digital data storage circuit - has one gate closed and second**

**and third gates alternately opened during testing and latches async. signals**

Patent Assignee: TEXAS INSTR INC ( **TEXI** ) ; TEXAS INSTR LTD ( **TEXI** )
Inventor: ROBRTSON I C; SIMPSON R D; ROBERTSON I C
Number of Countries: 002 Number of Patents: 004
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| GB 2220272 | A | 19900104 | GB 8815417 | A | 19880629 | 199001 B |
| US 4992727 | A | 19910212 | US 89373123 | A | 19890628 | 199109 |
| US 5122738 | A | 19920616 | US 89373123 | A | 19890628 | 199227 |
| | | | US 90594517 | A | 19901009 | |
| GB 2220272 | B | 19920930 | GB 8815417 | A | 19880629 | 199240 |

Priority Applications (No Type Date): GB 8815417 A 19880629
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| GB 2220272 | A | | 13 | | |
| US 5122738 | A | | 6 | G01R-031/28 | Div ex application US 89373123 |
| | | | | | Div ex patent US 4992727 |
| GB 2220272 | B | | 2 | G01R-031/28 | |

Abstract (Basic): GB 2220272 A

A testable digital data storage circuit has a gate connected to apply the voltage level established by a **switch** to the input of a first latch. Two other gates are respectively connected from a **test input** terminal to the input of the first latch and from the output of the first latch to the input of a second latch. The output of the second latch is connected to a test output terminal.

During normal operation, the first gate is maintained open to pass the voltage level to the first latch. During testing the first gate is closed and the second and third gate are opened alternately.

USE - Testing circuit in microprocessor and digital signal processor mfr.

32/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO


05278404 **Image available**
**BOUNDARY** SCANNING CIRCUIT

PUB. NO.: 08-233904 [JP 8233904 A]
PUBLISHED: September 13, 1996 (19960913)
INVENTOR(s): ABE YASUYUKI
APPLICANT(s): NEC ENG LTD [329822] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-037886 [JP 9537886]
FILED: February 27, 1995 (19950227)
INTL CLASS: [6] G01R-031/28; H01L-021/66; H01L-027/04; H01L-021/822
JAPIO CLASS: 46.2 (INSTRUMENTATION -- Testing); 42.2 (ELECTRONICS -- Solid State Components)

ABSTRACT

PURPOSE: To expedite testing by sequentially wiring the input and output terminals of a plurality of integrated circuits connecting them to starting and finishing ends, controlling a **switching** circuit and a selector, and selecting the wiring.

CONSTITUTION: Serial wirings C1, C2 in which a plurality of input and output terminals I and O of integrated circuits 10a to 10c are sequentially connected are used as output **boundary scan** buffers. **Switching** circuits 3a to 3c and selectors 4a, 4c are connected to the starting and finishing ends of the wirings C1, C2. At the time of serial testing, control circuits 50a to 50c control the circuits 3, 4 to select the wirings C1, C2. **Test data input** to the input terminal **TDI** of the circuit 10a is output from the output terminal **TDO** of the circuit 10c via input or output **boundary scan** buffers of the circuits 10a to 10c. Thus, as compared with the case that all the input and output terminals are scanned, a test can be executed in about a half as much time.

32/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO


04977894 **Image available**
INTEGRATED CIRCUIT DEVICE

PUB. NO.: 07-270494 [JP 7270494 A]
PUBLISHED: October 20, 1995 (19951020)
INVENTOR(s): NITTA SUSUMU
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-060995 [JP 9460995]
FILED: March 30, 1994 (19940330)
INTL CLASS: [6] G01R-031/28; H01L-021/66
JAPIO CLASS: 46.2 (INSTRUMENTATION -- Testing); 42.2 (ELECTRONICS -- Solid State Components)

ABSTRACT

PURPOSE: To shorten the testing time and restrain the occurrence of a delay time at the time of normal operation to the minimum by selectively applying one of signals from an internal **scan** circuit for the first selector means and a test path to the input side of the second selector means.

CONSTITUTION: A **scan - in** signal TD1 is sent to the input terminal of a **boundary scan** register 2 as well as to the input terminals A of **multiplexers** 3-1 to 3-n. **Scan - in** signals PSI1 to PSIn are sent to the input terminals B of the **multiplexers** 3-1 to 3-n. In this case, the

**multiplexers** 3-1 to 3-n select one of respective input signals, depending on a control signal PM and sends the selected signal to **scan** registers 1-1 to 1-n. Furthermore, a **multiplexer** 4 selects one of **scan - out** signals PSO1 to PSOn as output from the registers 1-1 to 1-n, and **scan - out** signal BSO as output from the register 2, and outputs the selected signal as test data **TDO** .

**32/5/3 (Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


015282253 **Image available**
WPI Acc No: 2003-343185/200332
XRPX Acc No: N03-274548
**Programming apparatus for programmable logic device, has processor and PLD modules connected to central host**
Patent Assignee: SIEMENS AG (SIEI )
Inventor: OTTE G
Number of Countries: 025 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| WO 200331997 | A2 | 20030417 | WO 2002DE3382 | A | 20020911 | 200332 B |
| EP 1432995 | A2 | 20040630 | EP 2002774331 | A | 20020911 | 200443 |
| | | | WO 2002DE3382 | A | 20020911 | |

Priority Applications (No Type Date): DE 12001047891 A 20010928
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200331997 | A2 | G | 11 | G01R-031/00 | |
| Designated States (National): US | | | | | |
| Designated States (Regional): AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR | | | | | |
| EP 1432995 | A2 | G | | G01R-031/3185 | Based on patent WO 200331997 |
| Designated States (Regional): AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SK TR | | | | | |

Abstract (Basic): WO 200331997 A2
NOVELTY - A **boundary scan** socket (BSS), a processor (MP) and at least one programmable device (PLD1...PLD4) are connected in a **boundary scan** chain via **boundary scan** connectors ( **TDI** , **TDO** , TMS, TCK). A **switch** device (SW) is provided so that the processor can be operatively connected as a transmitter and receiver for the **boundary scan** connections for the programmable devices.
USE - For complex systems such as communication **switching** system, in which programmable modules can be re-programmed (updated) via **scan boundary** devices by host.
ADVANTAGE - Eliminates need for local programming.
DESCRIPTION OF DRAWING(S) - The drawing shows an apparatus for testing the functionality of integrated devices in a module.
pp; 11 DwgNo 1/3
Title Terms: PROGRAM; APPARATUS; PROGRAM; LOGIC; DEVICE; PROCESSOR; MODULE; CONNECT; CENTRAL; HOST
Derwent Class: S01; T01; U21
International Patent Class (Main): G01R-031/00; G01R-031/3185
File Segment: EPI

**32/5/4 (Item 2 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


015281749 **Image available**
WPI Acc No: 2003-342681/200332
XRPX Acc No: N03-274082

**Electronic device has test interfaces for multiple subdevices coupled to form chain and test data out of last interface in chain and test data out of scan test interface coupled to bypass multiplexer**

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG ); LOUSBERG G E A (LOUS-I); VERMEULEN H G H (VERM-I); WAAYERS T F (WAAY-I)
Inventor: LOUSBERG G E A; VERMEULEN H G H; WAAYERS T F

Number of Countries: 034 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| WO 200325595 | A2 | 20030327 | WO 2002IB3617 | A | 20020904 | 200332 B |
| US 20030079166 | A1 | 20030424 | US 2002245489 | A | 20020917 | 200334 |
| EP 1430319 | A2 | 20040623 | EP 2002762683 | A | 20020904 | 200441 |
| | | | WO 2002IB3617 | A | 20020904 | |
| KR 2004035848 | A | 20040429 | KR 2004704092 | A | 20040319 | 200456 |
| JP 2005503563 | W | 20050203 | WO 2002IB3617 | A | 20020904 | 200516 |
| | | | JP 2003529172 | A | 20020904 | |
| CN 1555491 | A | 20041215 | CN 2002818281 | A | 20020904 | 200519 |

Priority Applications (No Type Date): EP 2001203565 A 20010920
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200325595 | A2 | E | 20 | G01R-031/00 | |
| Designated States (National): CN JP KR | | | | | |
| Designated States (Regional): AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR | | | | | |
| US 20030079166 | A1 | | | G01R-031/28 | |
| EP 1430319 | A2 | E | | G01R-031/3185 | Based on patent WO 200325595 |
| Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR | | | | | |
| KR 2004035848 | A | | | G01R-031/28 | |
| JP 2005503563 | W | | 42 | G01R-031/28 | Based on patent WO 200325595 |
| CN 1555491 | A | | | G01R-031/3185 | |


Abstract (Basic): WO 200325595 A2

NOVELTY - Electronic device (100) has subdevices (120a,120b), coupled to test interfaces (140a,140b). Test interfaces are arranged in chain (140) via **test data out** ( **TDO** ) of first interface (142a) coupled to **test data in** of next interface (141b). **Boundary scan** test interface (160) for testing other parts of device is coupled to start of chain. **TDO** of last interface (142b) in chain and **TDO** of **scan** test interface (162) are coupled to bypass **multiplexer** (102).

DETAILED DESCRIPTION - By coupling **TDO** of last interface in chain and **TDO** of **scan** test interface to bypass **multiplexer** , two possible routes from **test data input** (110) to **test data output** (112) are created; through the full chain or through test interface only.

USE - For PCBs carrying multiple subdevices, system-on chip architectures, multi-chip modules etc.

ADVANTAGE - Allows data to be provided to the subdevice test interfaces and a further test interface at the same time, thereby allowing a subdevice to be debugged while debug data is also provided to surrounding logic outwith the subdevice, thus enhancing fault coverage. The electronic device can be tested or debugged as a macro device or collection of devices.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of the electronic device.

Electronic device (100)
Bypass **multiplexer** (102)
**Test data input** (110)
**Test data output** (112)
Subdevices (120a,120b)
Chain (140)
Test interfaces (140a,140b)
**Test data in** of next interface (141b)
**Test data out** of first interface (142a)
**Test data out** of last interface (142b)

**Boundary scan** test interface (160)
**Test data out** of **boundary scan** test interface (162)
pp; 20 DwgNo 1/4
Title Terms: ELECTRONIC; DEVICE; TEST; INTERFACE; MULTIPLE; COUPLE; FORM; CHAIN; TEST; DATA; LAST; INTERFACE; CHAIN; TEST; DATA; **SCAN** ; TEST; INTERFACE; COUPLE; **MULTIPLEX**
Derwent Class: S01; U11; V04
International Patent Class (Main): G01R-031/00; G01R-031/28; G01R-031/3185
File Segment: EPI

**32/5/5 (Item 3 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014433114 **Image available**
WPI Acc No: 2002-253817/200230
XRPX Acc No: N02-195923
**Programmable** boundary scan **register for IEEE 1149.1 compliant programmable logic device, has bypass circuit to connect** test data input **terminal and output terminal of shift register to** test data output **terminal**
Patent Assignee: XILINX INC (XILI-N)
Inventor: CURD D R; JACOBSON N G
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6314539 | B1 | 20011106 | US 98176659 | A | 19981021 | 200230 | B |

Priority Applications (No Type Date): US 98176659 A 19981021
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6314539 | B1 | | 24 | G01R-031/28 | |

Abstract (Basic): US 6314539 B1
NOVELTY - A bypass circuit has a **multiplexer** (850) for selectively connecting a **test data input** terminal and a **test data output** terminal of a shift register (820) to a **test data output** terminal.
DETAILED DESCRIPTION - The shift register receives test data signal through the **test data input** terminal. The bypass circuit selectively connects the **test data input** terminal and the output terminal of the shift register to the **test data output** terminal. A parallel latch (830) selectively stores a predetermined test data signal received by the shift register. An output **multiplexer** (840) has its input terminals connected to the output terminal of the latch and a system data input terminal and its output terminal connected to a system data output terminal. A mode control circuit (860) selectively couples one of mode control signal and disable signal to a select terminal of the output multiplexer .
INDEPENDENT CLAIMS are also included for the following:
(a) Programmable input-output circuit;
(b) Programmable logic device.
USE - Programmable **boundary scan** register (BSR) in programmable input-output circuit of IEEE 1149.1 compliant programmable logic device (PLD) (claimed) including field programmable gate array (FPGA), and complex programmable logic device (CPLD) and other types of integrated circuits (ICs) used in electronic system.
ADVANTAGE - Since the bypass circuit directly passes data signals from the **test data input** terminals to the **test data output** terminal, selective removal of BSR cell from the BSR is enabled. Thereby allowing the user to adjust the length and change the configuration of the BSR, and the reduced length BSR facilitates faster **boundary scan** test procedures.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of

BSR cell.
Shift register (820)
Parallel latch (830)
Output **multiplexer** (840)
**Multiplexer** (850)
Mode control circuit (860)
pp; 24 DwgNo 8/12
Title Terms: PROGRAM; **BOUNDARY** ; **SCAN** ; REGISTER; COMPLIANT; PROGRAM; LOGIC; DEVICE; CIRCUIT; CONNECT; TEST; DATA; INPUT; TERMINAL; OUTPUT; TERMINAL; SHIFT; REGISTER; TEST; DATA; OUTPUT; TERMINAL
Derwent Class: S01; U11
International Patent Class (Main): G01R-031/28
File Segment: EPI

**32/5/6 (Item 4 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


012422701 **Image available**
WPI Acc No: 1999-228809/199919
XRPX Acc No: N99-169302
**Standard** boundary scan **interface extending method of IC**
Patent Assignee: BULL HN INFORMATION SYSTEMS INC (HONE )
Inventor: RUSSELL R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5887001 | A | 19990323 | US 95572252 | A | 19951213 | 199919 | B |
| | | | US 97946952 | A | 19971008 | | |

Priority Applications (No Type Date): US 95572252 A 19951213; US 97946952 A 19971008
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5887001 | A | | 21 | G01R-031/28 | Cont of application US 95572252 |

Abstract (Basic): US 5887001 A

NOVELTY - An analog control register (122) is operated in response to the instructions corresponding to the predetermined data bit pattern received through **TDI** terminal. The analog signal is transferred to the IC through TCK and TMS terminal to perform analog testing, based on output of register during phase operation determined by a phase control counter (153).

DETAILED DESCRIPTION - A control isolation **switch** (151) is connected between TMS and TCK terminals to input instructions to controller for operating the interface in analog and digital modes. The phase control counter is connected to the **TDI** terminal to receive external digital control signal, during analog mode and the counter outputs predetermined signals that determines predetermined phases of operation, based on whether the interface is operated either in analog or digital modes. The analog control register is connected to the **TDI** terminal and counter for receiving digital control signal displays predetermined phase. The sequencing phase of the IC terminal is controlled by connecting a **TDI** terminal to a **TDO** terminal through a **multiplexer** (118) based on signal generated by the register. The TMS and TCK terminals are connected to respective test and control points of IC through corresponding analog **switch** matrix (134,136). An analog control decoder (124) is connected to the **switch** matrix through another **switch** matrix (138). The decoder feeds predetermined data bit pattern for operating predetermined **switch** matrix. A reference voltage (140) is applied to the IC through the **switch** matrix (128), when the interface is operated at analog mode.

An INDEPENDENT CLAIM is included for apparatus for extending the capability of standard **boundary scan** interface of IC.

USE - For IC for processing analog and digital signals.
ADVANTAGE - Prevents interference by digital circuiting of digital block during analog measurements since control isolation **switch** is predetermined. Eliminates need to provide separate power since analog **switch** isolates certain system from other circuits during system power OFF.
DESCRIPTION OF DRAWING(S) - The figure shows block diagram of digital test system.
**Multiplexer** (118)
Analog control register (122)
Analog control decoder (124)
**Switch** matrix (128)
Analog **switch** matrix (134,136,138)
Reference voltage (140)
Control isolation **switch** (151)
Phase control counter (153)
pp; 21 DwgNo 1/9
Title Terms: STANDARD; **BOUNDARY** ; **SCAN** ; INTERFACE; EXTEND; METHOD; IC
Derwent Class: S01; U11; U13
International Patent Class (Main): G01R-031/28
File Segment: EPI

**32/5/7 (Item 5 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


012320363 **Image available**
WPI Acc No: 1999-126469/199911
XRPX Acc No: N99-092658
Boundary scan **register for wiring test of LSI board and function test of semiconductor device mounted on LSI board - has second** multiplexer **which outputs register output signal which is input into output buffer of input-output cell**
Patent Assignee: KAWASAKI STEEL CORP (KAWI )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 11002664 | A | 19990106 | JP 97156374 | A | 19970613 | 199911 | B |

Priority Applications (No Type Date): JP 97156374 A 19970613
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 11002664 | A | | 8 | G01R-031/28 | |

Abstract (Basic): JP 11002664 A
NOVELTY - A first **multiplexer** (12) selectively outputs the signal input to the input terminal of a semiconductor device via the input buffer (22a) of an input-output (I/O) cell (22), or a **scan - in** signal. A first flip-flop (14) holds the output of the first **multiplexer** and outputs a **scan - out** signal. The output of the first flip-flop is held by a second flip-flop (16). A second **multiplexer** (18) selectively outputs the signal input into the input terminal of the semiconductor device, or the output signal of the second flip-flop. The output of the second **multiplexer** is input into the output buffer (22b) of the I/O cell. DETAILED DESCRIPTION - The **boundary scan** register (10) is built in each semiconductor device mounted on a LSI board, and is provided corresponding to each input terminal of the semiconductor device. An invertor (20) inverts and outputs the output signal of the second **multiplexer** .
USE - For wiring test of LSI board and function test of semiconductor device mounted on LSI board.
ADVANTAGE - Maintains circuit scale of test circuit of **boundary scan** register even if number of input terminals of semiconductor device increases. Fault detection of **boundary scan** register can be

performed easily. DESCRIPTION OF DRAWING(S) - The figure shows the circuit diagram of the **boundary scan** register. (10) **boundary scan** register; (12) first **multiplexer** ; (14) first flip-flop; (16) second flip-flop; (18) second **multiplexer** ; (20) invertor; (22a) input buffer; (22b) output buffer; (22) input-output cell.

Dwg.1/4

Title Terms: **BOUNDARY** ; **SCAN** ; REGISTER; WIRE; TEST; LSI; BOARD; FUNCTION ; TEST; SEMICONDUCTOR; DEVICE; MOUNT; LSI; BOARD; SECOND; **MULTIPLEX** ; OUTPUT; REGISTER; OUTPUT; SIGNAL; INPUT; OUTPUT; BUFFER; INPUT; OUTPUT; CELL

Derwent Class: S01; T01

International Patent Class (Main): G01R-031/28

International Patent Class (Additional): G06F-011/22

File Segment: EPI

**32/5/8 (Item 6 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



012239887 **Image available**

WPI Acc No: 1999-045995/199904

Related WPI Acc No: 1999-045996; 1999-070854

XRPX Acc No: N99-033497

Boundary scan **element and communication device - uses input and output terminal side** boundary **cells connected in parallel between** test data in **and** test data out **terminals**

Patent Assignee: KOKEN KK (KOKE ); NAGOYA M (NAGO-I); DUAKISHIZ KK (DUAK-N)

Inventor: NAGOYA M

Number of Countries: 022 Number of Patents: 011

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 9855926 | A1 | 19981210 | WO 98JP2383 | A | 19980529 | 199904 | B |
| EP 987632 | A1 | 20000322 | EP 98921883 | A | 19980529 | 200019 | |
| | | | WO 98JP2383 | A | 19980529 | | |
| JP 11502040 | X | 20001219 | WO 98JP2383 | A | 19980529 | 200104 | |
| | | | JP 99502040 | A | 19980529 | | |
| KR 2001013021 | A | 20010226 | KR 99710996 | A | 19991126 | 200154 | |
| KR 2001013200 | A | 20010226 | KR 99711187 | A | 19991130 | 200154 | |
| KR 2001013201 | A | 20010226 | KR 99711188 | A | 19991130 | 200154 | |
| KR 315999 | B | 20011212 | WO 98JP2432 | A | 19980602 | 200247 | |
| | | | KR 99711188 | A | 19991130 | | |
| KR 316000 | B | 20011212 | WO 98JP2404 | A | 19980601 | 200247 | |
| | | | KR 99710996 | A | 19991126 | | |
| US 6658614 | B1 | 20031202 | WO 98JP2383 | A | 19980529 | 200379 | |
| | | | US 99424454 | A | 19991123 | | |
| CA 2485309 | A1 | 19981210 | CA 2291681 | A | 19980529 | 200511 | |
| | | | CA 2485309 | A | 19980529 | | |
| KR 454989 | B | 20041106 | WO 98JP2383 | A | 19980529 | 200517 | |
| | | | KR 99711187 | A | 19991130 | | |

Priority Applications (No Type Date): JP 97143804 A 19970602

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 9855926 | A1 | J | 35 | G06F-011/22 | |
| Designated States (National): CA JP KR US | | | | | |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE | | | | | |
| EP 987632 | A1 | E | | G06F-011/22 | Based on patent WO 9855926 |
| Designated States (Regional): DE FR GB IT | | | | | |
| JP 11502040 | X | | | G06F-011/22 | Based on patent WO 9855926 |
| KR 2001013021 | A | | | G06F-011/22 | |
| KR 2001013200 | A | | | G01R-031/28 | |
| KR 2001013201 | A | | | G06F-011/22 | |

| | | | |
|---|---|---|---|
| KR 315999 | B | G06F-011/22 | Previous Publ. patent KR 2001013201<br>Based on patent WO 9855927 |
| KR 316000 | B | G06F-011/22 | Previous Publ. patent KR 2001013021<br>Based on patent WO 9858317 |
| US 6658614 | B1 | G01R-031/28 | Based on patent WO 9855926 |
| CA 2485309 | A1 E | H04L-012/26 | Div ex application CA 2291681 |
| KR 454989 | B | G01R-031/28 | Previous Publ. patent KR 2001013200<br>Based on patent WO 9855926 |

Abstract (Basic): WO 9855926 A

The **scan** element includes a number of input terminal side **boundary** cells allocated individually to respective input terminals and connected in series. A number of output terminal side **boundary** cells is allocated individually to respective output terminals and connected in series. A TAP circuit is used for controlling the input of data to the input terminal side **boundary** cells and the output from the output terminal side **boundary** cells. A **test data in** ( **TDI** ) terminal is provided for inputting serial data to be fed to the **boundary** cells. A **test data out** ( **TDO** ) terminal is used for outputting data from the **boundary** cells as serial data.

A test clock (TCK) terminal is used to which a clock signal is inputted. A test mode select (TMS) terminal is used for inputting a mode signal for **switching** the operation mode of the TAP circuit. The input and output terminal side **boundary** cells are connected in parallel between the **TDI** terminal and the **TDO** terminal.

Dwg.2/10

Title Terms: **BOUNDARY** ; **SCAN** ; ELEMENT; COMMUNICATE; DEVICE; INPUT; OUTPUT; TERMINAL; SIDE; **BOUNDARY** ; CELL; CONNECT; PARALLEL; TEST; DATA; TEST; DATA; TERMINAL

Derwent Class: S01; T01
International Patent Class (Main): G01R-031/28; G06F-011/22; H04L-012/26
International Patent Class (Additional): G01R-031/28
File Segment: EPI

32/5/9 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX


012239886 **Image available**
WPI Acc No: 1999-045994/199904
XRPX Acc No: N99-033496

**Communication equipment - has communication controller that transmits and receives control data for individually controlling terminals via boundary scanning elements**

Patent Assignee: KOKEN KK (KOKE ); NAGOYA M (NAGO-I); DUAKISHIZ KK (DUAK-N); DUAXES CORP (DUAX-N)
Inventor: NAGOYA M
Number of Countries: 022 Number of Patents: 007
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| WO 9855925 | A1 | 19981210 | WO 98JP2356 | A | 19980528 | 199904 B |
| EP 987631 | A1 | 20000322 | EP 98921861 | A | 19980528 | 200019 |
| | | | WO 98JP2356 | A | 19980528 | |
| JP 11502036 | X | 20001219 | WO 98JP2356 | A | 19980528 | 200104 |
| | | | JP 99502036 | A | 19980528 | |
| KR 2001013017 | A | 20010226 | KR 99710991 | A | 19991126 | 200154 |
| KR 316001 | B | 20011212 | WO 98JP2356 | A | 19980528 | 200247 |
| | | | KR 99710991 | A | 19991126 | |
| CA 2291692 | C | 20030520 | CA 2291692 | A | 19980528 | 200335 |
| | | | WO 98JP2356 | A | 19980528 | |
| US 6591387 | B1 | 20030708 | WO 98JP2356 | A | 19980528 | 200353 |
| | | | US 99424452 | A | 19991123 | |

Priority Applications (No Type Date): JP 97143809 A 19970602
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 9855925 | A1 | J | 29 | G06F-011/22 | |
| Designated States (National): CA JP KR US | | | | | |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE | | | | | |
| EP 987631 | A1 | E | | G06F-011/22 | Based on patent WO 9855925 |
| Designated States (Regional): DE FR GB IT | | | | | |
| JP 11502036 | X | | | G06F-011/22 | Based on patent WO 9855925 |
| KR 2001013017 | A | | | G06F-011/22 | |
| KR 316001 | B | | | G06F-011/22 | Previous Publ. patent KR 2001013017 Based on patent WO 9855925 |
| CA 2291692 | C | E | | G06F-011/22 | Based on patent WO 9855925 |
| US 6591387 | B1 | | | G01R-031/28 | Based on patent WO 9855925 |

Abstract (Basic): WO 9855925 A

The equipment is composed of a number of **boundary** cells respectively assigned to input terminals and output terminals. A TAP circuit controls the data input to and output from the **boundary** cells. a number of **boundary** scanning elements is provided with **test data in** ( **TDI** ) terminals for inputting serial data to be given to the **boundary** cells. **Test data out** ( **TDO** ) terminals are used for outputting the data from the **boundary** cells as serial data. Test clock (TCK) terminals are used for inputting clock signals. Test mode select (TMS) terminals are provided for inputting mode signals for **switching** the operational mode of the TAP circuit.

A number of terminals having ICs which are respectively connected to or incorporated with the **boundary** scanning elements. A communication controller is connected to the **boundary** scanning elements in series and transmits and receives control data for individually controlling the terminals through the **boundary** scanning elements. A data communication line is connected to the terminals in parallel through which the output data of the terminals are sent to the communication controller.

Dwg.1/9

Title Terms: COMMUNICATE; EQUIPMENT; COMMUNICATE; CONTROL; TRANSMIT; RECEIVE; CONTROL; DATA; INDIVIDUAL; CONTROL; TERMINAL; **BOUNDARY** ; **SCAN** ; ELEMENT
Derwent Class: T01
International Patent Class (Main): G01R-031/28; G06F-011/22
International Patent Class (Additional): G06F-011/22
File Segment: EPI

**32/5/10 (Item 8 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


011335447 **Image available**
WPI Acc No: 1997-313352/199729
XRPX Acc No: N97-259453
**Driver integrated circuit chip for controlling data and signals flowing to print-head of non-impact printer - selects test and control data from output of** test data output **terminal, using registers connected to** test data input **terminal**
Patent Assignee: EASTMAN KODAK CO (EAST ); NEXPRESS SOLUTIONS LLC (NEXP-N)
Inventor: DONAHUE M J; FLEMING P J; FOX T; KELLY E M; MATTERN M W; PETRUZELLI C M; FLEMMING P J
Number of Countries: 004 Number of Patents: 005
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| GB 2308664 | A | 19970702 | GB 9626392 | A | 19961219 | 199729 | B |
| DE 19654135 | A1 | 19970703 | DE 1054135 | A | 19961223 | 199732 | |
| JP 9207383 | A | 19970812 | JP 96355519 | A | 19961203 | 199742 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| US 5859657 | A | 19990112 | US 95581025 | A | 19951228 | 199910 | |
| GB 2308664 | B | 20001101 | GB 9626392 | A | 19961219 | 200056 | |

Priority Applications (No Type Date): US 95581025 A 19951228
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| GB 2308664 | A | | 73 | G01R-031/28 | |
| DE 19654135 | A1 | | 38 | H04N-001/032 | |
| JP 9207383 | A | | 102 | B41J-002/44 | |
| US 5859657 | A | | | B41J-002/47 | |
| GB 2308664 | B | | | G01R-031/28 | |

Abstract (Basic): GB 2308664 A

The driver IC chip has a driver incorporating current-carrying channels carrying current to respective recording elements on a printhead, and a controller for operating the driver. The controller includes a circuit for providing a test circuit interface having : a test access port for input of update command signals and clock inputs to the test circuit, a test data input terminal for inputting test data and control data into the chip, and registers connected to the test data input terminal for storing control data for operating the driver, and a **test data output** terminal for outputting test data and control data from the chip to an adjacent chip.

A selector connected to the first registers and the test data output terminal selects test and control data for output from the **test data output** terminal. The selector includes an instruction register for storing instructions for selecting one of the first registers for receiving data from the test data input terminal and for selecting one of the registers for outputting data from one of the first registers via a **multiplexer** for controlling the driver.

ADVANTAGE - Enables access to certain registers e.g. LREF and GREF at any time without interrupting normal image data loading and printing operation, and access to additional control functions on driver chips, without need of dedicated secondary data path on driver chip and while still providing standard IEEE 1149.1 testability functions inc. **boundary scan** . Provides control data for control functions without affecting printing.

Dwg.11/19

Title Terms: DRIVE; INTEGRATE; CIRCUIT; CHIP; CONTROL; DATA; SIGNAL; FLOW; PRINT; HEAD; NON; IMPACT; PRINT; SELECT; TEST; CONTROL; DATA; OUTPUT; TEST; DATA; OUTPUT; TERMINAL; REGISTER; CONNECT; TEST; DATA; INPUT; TERMINAL
Derwent Class: P75; S01; T01; T04; U11; V04
International Patent Class (Main): B41J-002/44; B41J-002/47; G01R-031/28; H04N-001/032
International Patent Class (Additional): B41J-002/435; B41J-002/45; B41J-002/455; G06F-011/00; G06F-011/22
File Segment: EPI; EngPI

**32/5/11 (Item 9 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


010418860 **Image available**
WPI Acc No: 1995-320175/199541
XRPX Acc No: N95-240871
**Integrated circuit test access port - has instruction register coupled to multiplexer and controller with application of first instruction causing multiplexer to select and maintain path between test data input and output lines**
Patent Assignee: BULL HN INFORMATION SYSTEMS INC (HONE )

Inventor: RUSSELL R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5448576 | A | 19950905 | US 92968104 | A | 19921029 | 199541 | B |

Priority Applications (No Type Date): US 92968104 A 19921029
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5448576 | A | | 18 | H04B-017/00 | |

Abstract (Basic): US 5448576 A

The port includes a number of register-like transfer circuits, each having an input and an output. The input of each is connected to a **test data input** line ( **TDI** )and the output to a different, predetermined **multiplexer** input (0-5). An instruction register (106) stores information pertaining to any one of a number of instructions coded and generating signals defining a number of operational modes.

The instruction register is coupled to the **multiplexer** (118) and to the controller, and in response to application of a first instruction by the **test data input** causes the **multiplexer** to select and during testing maintain the selected as a path between the **test data input** and output lines ( **TDO** ). The transfer circuits effectively provides a minimum length shift path to minimise the number of bits required to be shifted through a string of IC devices to carry out the testing.

ADVANTAGE - Minimises number of bits serially scanned into device controllers by temporarily disabling paths not required.. Allows continuous verification of inoperative state of test logic and diagnosis of test logic faults. Decreases amount of external hardware required. Minimises overall **boundary scan** chain bit length and dependency on clocking for shift operations.

Dwg.1A/6

Title Terms: INTEGRATE; CIRCUIT; TEST; ACCESS; PORT; INSTRUCTION; REGISTER; COUPLE; **MULTIPLEX** ; CONTROL; APPLY; FIRST; INSTRUCTION; CAUSE; **MULTIPLEX** ; SELECT; MAINTAIN; PATH; TEST; DATA; INPUT; OUTPUT; LINE
Derwent Class: S01; U11; U21
International Patent Class (Main): H04B-017/00
File Segment: EPI

**32/5/12 (Item 10 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


010340003 **Image available**
WPI Acc No: 1995-242085/199532
XRPX Acc No: N95-188699

Boundary - Scan **-compliant multi-chip module - has number of semiconductor chips in chain each having Test Data Inputs and Test Data Outputs to pass stream of test information bits and has by-pass circuit to be** boundary scan **compliant**

Patent Assignee: AT & T CORP (AMTT ); AMERICAN TELEPHONE & TELEGRAPH CO (AMTT ); LUCENT TECHNOLOGIES INC (LUCE )
Inventor: JARWALA N T; YAU C W
Number of Countries: 010 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 662616 | A2 | 19950712 | EP 94309103 | A | 19941207 | 199532 | B |
| TW 253031 | A | 19950801 | TW 94109588 | A | 19941015 | 199540 | |
| JP 7287053 | A | 19951031 | JP 94336988 | A | 19941227 | 199601 | |
| US 5673276 | A | 19970930 | US 93172778 | A | 19931227 | 199745 | |
| | | | US 96716559 | A | 19960205 | | |
| JP 3096597 | B2 | 20001010 | JP 94336988 | A | 19941227 | 200052 | |
| KR 208306 | B1 | 19990715 | KR 9437123 | A | 19941227 | 200066 | |

Priority Applications (No Type Date): US 93172778 A 19931227; US 96716559 A 19960205
Cited Patents: No-SR.Pub
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 662616 | A2 | E | 12 | G01R-031/28 | |
| Designated States (Regional): DE ES FR GB IT NL | | | | | |
| TW 253031 | A | | | G01R-031/26 | |
| JP 7287053 | A | | 12 | G01R-031/28 | |
| US 5673276 | A | | 11 | H04B-017/00 | Cont of application US 93172778 |
| JP 3096597 | B2 | | 13 | G01R-031/28 | Previous Publ. patent JP 7287053 |
| KR 208306 | B1 | | | G01R-031/28 | |

Abstract (Basic): EP 662616 A

The module (10) includes a number of semiconductor chips (141-14n) with each chip having a **Boundary Scan** architecture with a **Test Data Input** so that the chip can receive a stream of test information bits (including instructions and test data). When the stream of test information bits have passed through the chip, they appear at it's **Test Data Output** . The chips are coupled in a **Boundary - Scan** chain so that the initial chip receives signals at its **TDI** via the **TDI** module.

The last chip in the chain supplies signals from its **TDO** to the **TDO** of the module. Each chip in the chain has its **TDI** coupled to the **TDO** of an upstream chip. A bypass circuit (36') causes the stream of test input bits to be bypassed directly from the **TDI** to the **TDO** during selected intervals so that the chips appear as a single **Boundary - Scan** -compliant device during the interval.

USE/ADVANTAGE - Multichip module can be tested using **Boundary Scan** test technique. MCM can be tested as circuit board or as single device using **Boundary scan** test technique. **Boundary scan** circuit enables testing according to IEEE standard 1149.1.

Dwg.3/10

Title Terms: **BOUNDARY** ; **SCAN** ; COMPLIANT; MULTI; CHIP; MODULE; NUMBER; SEMICONDUCTOR; CHIP; CHAIN; TEST; DATA; INPUT; TEST; DATA; OUTPUT; PASS; STREAM; TEST; INFORMATION; BIT; BY-PASS; CIRCUIT; **BOUNDARY** ; **SCAN** ; COMPLIANT
Derwent Class: S01; T01; U11
International Patent Class (Main): G01R-031/26; G01R-031/28; H04B-017/00
International Patent Class (Additional): G06F-011/22; G06F-011/26; H01L-021/66
File Segment: EPI

**32/5/13 (Item 11 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


010245783 **Image available**
WPI Acc No: 1995-147038/199519
XRPX Acc No: N95-115457

**Boundary scan interface extension method for IC - by including circuits enabling sharing of data paths at separate time intervals defined under instruction control for processing analog and digital signals**

Patent Assignee: BULL HN INFORMATION SYSTEMS INC (HONE )
Inventor: RUSSELL R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5404358 | A | 19950404 | US 9313464 | A | 19930204 | 199519 | B |

Priority Applications (No Type Date): US 9313464 A 19930204
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|

US 5404358 A 18 G06F-015/20

Abstract (Basic): US 5404358 A

The method allows analog and digital signal processing by extending the interface with analog test circuits. The analog test circuits (126,132,128,134,136,138) share the interface data pins. The pins are digital data input ( **TDI** ) terminal and digital data output ( **TDO** ). They are shared by time allocation. The digital control section (150) generates control signals specifying the mode of operation. It generates enabling signals for connecting **TDI** and **TDO** pins.

When the digital test circuitry is activated by the interface test clock signal (TCK) the analog test circuits are disabled. The digital test operates until all data are passed. The interface test mode select (TMS) pin and clock (TCK) control the passing of data. Analog data is loaded into the analog control register. It is then loaded into the instruction register. When the instruction is decoded the analog mode is activated. The analog **switches** in the IC connect the analog measurement circuits of the tester to the **TDI** , **TDO** pins for analog measurement.

USE/ADVANTAGE - For ICs esp. circuits with standard **boundary scan** test access port. Provides hybrid capability without increase in interface lines, analog interface without detriment to digital scanning techniques.

Dwg.1/7

Title Terms: **BOUNDARY** ; **SCAN** ; INTERFACE; EXTEND; METHOD; IC; CIRCUIT; ENABLE; SHARE; DATA; PATH; SEPARATE; TIME; INTERVAL; DEFINE; INSTRUCTION; CONTROL; PROCESS; ANALOGUE; DIGITAL; SIGNAL

Derwent Class: T01; U11

International Patent Class (Main): G06F-015/20

File Segment: EPI

**32/5/14 (Item 12 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



010175329 **Image available**

WPI Acc No: 1995-076582/199511

Related WPI Acc No: 1992-399183

XRPX Acc No: N95-060826

**Pin** multiplexing **for programming and testing IC's - has IC with in system programming and** boundary scan **testing ability sharing same pins with one dedicated pin to select mode of operation**

Patent Assignee: LATTICE SEMICONDUCTOR CORP (LATT-N)

Inventor: CHAN A L; SHANKAR K; SHEN J; TSUI C Y

Number of Countries: 005 Number of Patents: 005

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 639006 | A1 | 19950215 | EP 94202212 | A | 19940728 | 199511 | B |
| US 5412260 | A | 19950502 | US 91695356 | A | 19910503 | 199523 | |
| | | | US 93106263 | A | 19930813 | | |
| JP 7175677 | A | 19950714 | JP 94211922 | A | 19940812 | 199537 | |
| EP 639006 | B1 | 20031022 | EP 94202212 | A | 19940728 | 200373 | |
| DE 69433259 | E | 20031127 | DE 633259 | A | 19940728 | 200403 | |
| | | | EP 94202212 | A | 19940728 | | |

Priority Applications (No Type Date): US 93106263 A 19930813; US 91695356 A 19910503

Cited Patents: US 5237218; WO 9220157

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 639006 | A1 | E | 16 | H03K-019/173 | |
| Designated States (Regional): DE GB IT | | | | | |
| US 5412260 | A | | 13 | H03K-019/003 | CIP of application US 91695356 |
| | | | | | CIP of patent US 5237218 |

JP 7175677 A 14 G06F-011/22
EP 639006 B1 E H03K-019/173
Designated States (Regional): DE GB IT
DE 69433259 E H03K-019/173 Based on patent EP 639006

Abstract (Basic): EP 639006 A
The high density programmable logic device includes both **boundary scan** testing and in-system programming facilities. The device uses five pins to perform either function. One pin (1) is used to select whether programming or testing is to be performed. The other four pins have different uses in each mode.
Within the device an input **multiplexer** (12) decodes the three common input pins (2-4) depending upon the control pin (ISPEN). The output (5) is decoded (14) by another **multiplexer** . The device has two state machines which control programming (16) or **boundary scan** testing (18).
ADVANTAGE - Economises on the number of pins required to perform both programming and testing functions.
Dwg.4/6
Title Terms: PIN; **MULTIPLEX** ; PROGRAM; TEST; IC; IC; SYSTEM; PROGRAM; **BOUNDARY** ; **SCAN** ; TEST; ABILITY; SHARE; PIN; ONE; DEDICATE; PIN; SELECT; MODE; OPERATE
Derwent Class: S01; U11; U13; U21
International Patent Class (Main): G06F-011/22; H03K-019/003; H03K-019/173
International Patent Class (Additional): G01R-031/28
File Segment: EPI

**32/5/15 (Item 13 from file: 350)**


009025786 **Image available**
WPI Acc No: 1992-153146/199219
XRPX Acc No: N92-114277
**Integrated circuit with intrinsic** boundary scan **test facility - has all terminals available to series-connected test loop through** multiplexers **which are themselves monitored**
Patent Assignee: THOMSON COMPOSANTS (CSFC )
Inventor: LESTRAT P
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| FR 2666902 | A | 19920320 | FR 9011491 | A | 19900918 | 199219 | B |

Priority Applications (No Type Date): FR 9011491 A 19900918
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| FR 2666902 | A | | 20 | | |

Abstract (Basic): FR 2666902 A
A **boundary scan** register links each input (10) with the series-connected test loop( **tdi** / **tdo** ). One **multiplexer** ( **MUX** ,16) takes inputs from either side of another ( **MUX** ,18), in the main circuit (10-14), and a third input from the adjoining register( **tdi** ). One of these is selected as output to a time-controlled(H1) flip-flop (20) by centrally provided signals(CTRL1,CTRL1A).
The flip-flop output continues to the following register ( **tdo** ), and, through a second time-controlled(H2) flip-flop, provides a second input to the first muiltiplexer ( **MUX** ,18), controlled by another central signal(CTRL2). Output and bi-directional terminals are similarly equipped.

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         (c) 1998 Inst for Sci Info
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File  62:SPIN(R) 1975-2005/Feb W4
         (c) 2005 American Institute of Physics
File 239:Mathsci 1940-2005/Jun
         (c) 2005 American Mathematical Society

Set     Items   Description
S1      13398   "TEST"()DATA()(IN OR INPUT) OR TDI OR SCAN()IN
S2        525   "TEST"()DATA()(OUT OR OUTPUT) OR TDO OR SCAN()OUT
S3     254777   (INPUT OR NORMAL)()DATA OR DATA()IN
S4     194778   MULTIPLEX??? OR MULTIPLEX??? OR MUX???
S5      16911   DEMULTIPLEX??? OR DEMULTIPLEX??? OR DMUX??? OR DEMUX???
S6     727048   SWITCH???
S7     181054   SCAN
S8     380358   CAPTUR???
S9    2535760   RESPONSE
S10     16316   (SECOND OR 2ND)(3W)S4:S6 OR S4:S6(2W)(TWO OR 2)
S11         0   S1 AND S2 AND S10 AND S7
S12         0   S1:S2 AND S10 AND S7
S13         0   S1 AND S2 AND S4 AND S5 AND S7
S14         2   S1 AND S2 AND S4 AND S7
S15         4   S1:S2 AND S4:S5 AND S7 AND S8:S9
S16         6   S14:S15
S17         3   RD (unique items)
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17/5/1 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online


1060062 ORDER NO: AADDX-84995
**AN INVESTIGATION INTO THE REALISATION AND TESTING OF A UNIVERSAL LOGIC PRIMITIVE GATE ARRAY**
Author: CHENGJIN, ZHANG
Degree: PH.D.
Year: 1988
Corporate Source/Institution: UNIVERSITY OF BATH (UNITED KINGDOM) (0690)
Source: VOLUME 50/02-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 639. 382 PAGES
Descriptors: COMPUTER SCIENCE; ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0984; 0544

Available from UMI in association with The British Library.
In this thesis, an investigation is described which was carried out into the realisation and testing of a universal logic primitive gate array.
During this study, a new gate array with a more powerful logic primitive, the **multiplexer** , has been proposed. The CMOS transmission gate has been used to implement this primitive. With it, any logic circuits, including combinational and sequential circuits, can be easily realised. The synthesis can be achieved by either the modular tree structure or unrestricted topologies. Spectral techniques have been used as one of the logic design techniques to improve the design of **multiplexer** universal logic module circuits.
The placement and routing of this gate array have been considered. For the ease of routing, the linear topology has been adopted, and two terminals to the basic cell have been provided. The comparison between single metal and double metal layers for customisation has been made through the whole design of the layout.
The common faults in digital systems, such as stuck-at faults, bridging faults and CMOS open faults, have been discussed and analysed. Some relationships between stuck-at faults and bridging faults, have been studied and it has been shown that some bridging faults, like input bridging faults and feedback bridging faults, could be detected by stuck-at fault test sets.
The diagnosis of faults in the modular tree structure has been discussed. Providing more test sets, stuck-at faults can be located easily, the detection of stuck-at faults can be done quickly by the test sets formed by two matrices.
The structured design for testing in this gate array has been considered. The partitioning and **scan in scan out** design techniques have been used to increase the testability. A proposed built-in test for this gate array has been given.
Throughout the study, all the efforts have been made towards searching for a gate array design which could give a good opportunity for customisation and fault detection in LSI systems.

17/5/2 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC


6041721 INSPEC Abstract Number: B9811-1265B-110, C9811-5210B-052
**Title: A design-for-testability technique for register-transfer level circuits using control/data flow extraction**
Author(s): Ghosh, I.; Raghunathan, A.; Jha, N.K.
Author Affiliation: Dept. of Electr. Eng., Princeton Univ., NJ, USA
Journal: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems vol.17, no.8 p.706-23
Publisher: IEEE,
Publication Date: Aug. 1998 Country of Publication: USA

CODEN: ITCSDI ISSN: 0278-0070
SICI: 0278-0070(199808)17:8L.706:DTTR;1-E
Material Identity Number: B959-98014
U.S. Copyright Clearance Center Code: 0278-0070/98/$10.00
Document Number: S0278-0070(98)05824-2
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Theoretical (T); Experimental (X)

Abstract: In this paper, we present a technique for extracting functional (control/data flow) information from register-transfer level controller/data path circuits, and illustrate its use in design for hierarchical testability of these circuits. This scheme does not require any additional behavioral information. It identifies a suitable control and data flow from the register-transfer level circuit, and uses it to test each embedded element in the circuit by symbolically justifying its precomputed test set from the system primary inputs to the element inputs and symbolically propagating the output **response** to the system primary outputs. When symbolic justification and propagation become difficult, it inserts test **multiplexers** at suitable points to increase the symbolic controllability and observability of the circuit. These test **multiplexers** are mostly restricted to off-critical paths. Testability analysis and insertion are completely based on the register-transfer level circuit and the functional information automatically extracted from it, and are independent of the data path bit width owing to their symbolic nature. Furthermore, the data path test set is obtained as a byproduct of this analysis without any further search. Unlike many other design-for-testability techniques, this scheme makes the combined controller-data path very highly testable. It is general enough to handle control-flow-intensive register-transfer level circuits like protocol handlers as well as data-flow intensive circuits like digital filters. It results in low area/delay/power overheads, high fault coverage, and very low test generation times (because it is symbolic and independent of bit width). Also, a large part of our system-level test sets can be applied at speed. Experimental results on many benchmarks show the average area, delay, and power overheads for testability to be 3.1, 1.0, and 4.2%, respectively. Over 99% fault coverage is obtained in most cases with two-four orders of magnitude test generation time advantage over an efficient gate-level sequential test pattern generator and one-three orders of magnitude advantage over an efficient gate-level combinational test pattern generator (that assumes full **scan** ). **In** addition, the test application times obtained for our method are comparable with those of gate-level sequential test pattern generators, and up to two orders of magnitude smaller than designs using full **scan** . (37 Refs)

Subfile: B C

Descriptors: automatic testing; data flow graphs; design for testability; fault diagnosis; logic testing; sequential circuits

Identifiers: design-for-testability technique; register-transfer level circuits; control/data flow extraction; hierarchical testability; embedded element; precomputed test set; system primary inputs; symbolic justification; test **multiplexers** ; symbolic controllability; symbolic observability; off-critical paths; protocol handlers; area/delay/power overheads; fault coverage; test generation times; sequential test

Class Codes: B1265B (Logic circuits); B0250 (Combinatorial mathematics); B7210B (Automatic test and measurement systems); C5210B (Computer-aided logic design); C1160 (Combinatorial mathematics); C7410D (Electronic engineering computing); C5120 (Logic and switching circuits)



**17/5/3 (Item 1 from file: 95)**
DIALOG(R)File 95:TEME-Technology & Management


01205075 E98050550212
**Testing embedded memory array using unified** scan **path**
(Pruefen eingebetteter Speicher-Arrays unter Verwendung eines einheitlichen

Abtastpfades)
Yano, S
NEC Corp., J
NEC Research and Development, v39, n1, pp14-25, 1998
Document type: journal article  Language: English
Record type: Abstract
ISSN: 0547-051X

ABSTRACT:
The authors have previously proposed a scannable memory configuration, which makes ordinary memory arrays to operate as virtual **scan** registers by adding a small support circuit. It allows incorporation of both memory arrays and flip-flops in a single **scan** path. Automatic test pattern generation for combinational circuits can thus be used to generate test pattern for sequential circuits composed of memory arrays and random logic. From the viewpoint of memory testing, this paper investigates the testability of the scannable memory configuration and proposes a memory array test using the **scan** path. Simply by comparing **scan - in** data and **scan - out** data, the test can detect memory specific faults such as coupling faults between memory cells as well as stuck-at faults. The test vector is 20 x m + s bit long, where m is the number of words of the memory array under test and s is the total **scan** path length.